Confidentiality level: external use

UM800YA User Manual

V1.0.2

Unicmicro (Guangzhou) Co., Ltd.

http://www.unicmicro.com/

Copyright & Disclaimer

Contents

List of Figures

List of Tables

1 Overview

The UM800YA is a general-purpose MCU with 1T 8051 core. It runs faster and offers superior performance compared to traditional 8051 MCUs under the same system clock, while maintaining full compatibility with traditional 8051 instruction code.

1.1 Main Features

- 8-bit microcontroller based on the 1T 8051 instruction pipeline structure
- eFlash: up to 64 KB (supporting IAP)
- RAM: Idata of 256 bytes, and Xdata up to 4096 bytes
- Operating voltage: 2.5 V–5.5 V
- Clock sources
  - Internal RCH: 16 MHz
  - Internal RCL: 38 kHz
  - External clock input: < 16 MHz
  - Crystal resonator: < 16 MHz
- 17 bidirectional CMOS I/O pins (with built-in pull-up/pull-down resistors)
- Up to 3 GTIMERs, supporting input capture and complementary PWM with dead-time insertion
- Up to 11 × 16-bit PWM outputs
- 1 x LPTIMER, each supporting 2 input captures and 2 PWM outputs
- 4 x UARTs: UART0 / UART1 / UART2 / UART3
- 1 x SPI, supporting master and slave modes
- 8 external channels, 1 MSPS, 12-bit ADC @ 3 V

- Watchdog timer (WDT)
- Buzzer generator
- Interrupt sources
  - EFC interrupt
  - External interrupt supported on all IO pins
  - UART0/UART1/UART2/UART3
  - ADC
  - PWM period interrupt
  - SPI
  - I2C
  - LPTIMER
  - GTIMER
- Reset sources
  - POR (power-on reset)
  - LVR (low-voltage reset)
  - LVD (low-voltage detection)
  - Watchdog reset
  - Pin reset
- Built-in LVD module
- Power-saving modes
  - Typical current in Stop mode: 0.75 μA
  - Typical current in DeepSleep mode: 1.1 μA
  - Typical current in Sleep mode: 245 μA
  - Typical current in Active mode: 80 μA/MHz

1.2 Functional Block Diagram

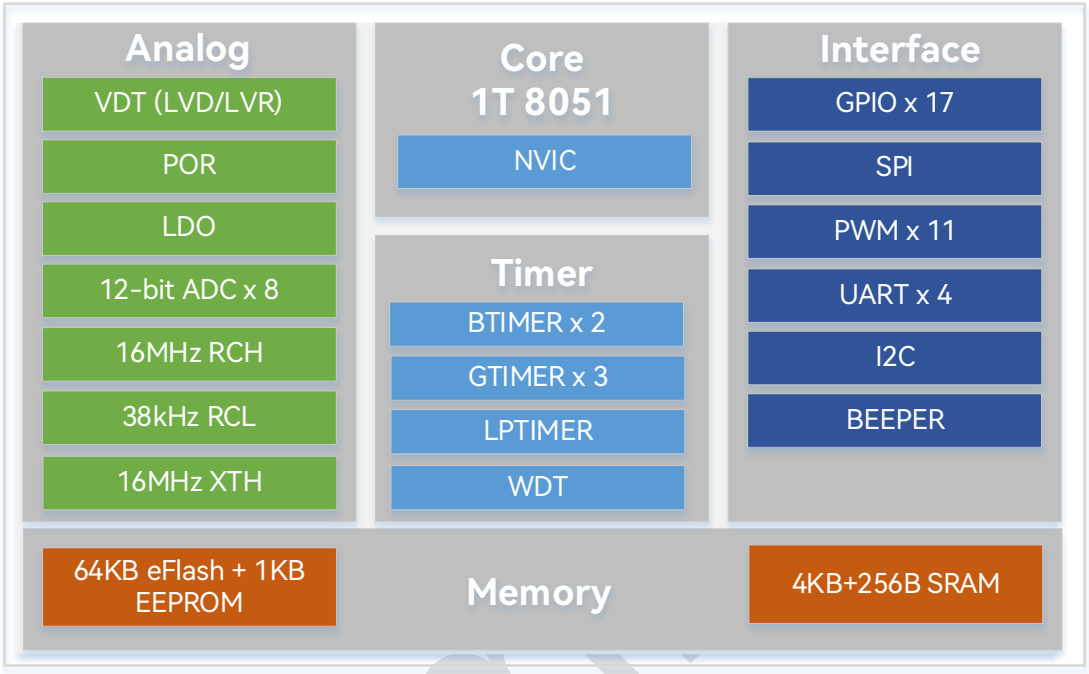


Figure 1-1: Chip Functional Diagram

2 Processor

2.1 Main Features

CPU core registers: ACC, B, PSW, SP, DPS, DPL, DPH, DPL1, DPH1.

2.2 Program Status Word (PSW) Register

The PSW register contains program status information.

2.3 Accumulator (ACC)

The accumulator is a commonly used dedicated register, which is often used to store operands involved in operations and the operation results.

2.4 B Register

The B register is used in multiplication and division instructions. In other instructions, it can be used as a general-purpose temporary register.

2.5 Data Pointer (DPTR)

The data pointer (DPTR) is a 16-bit dedicated register, with the high-byte register denoted as DPH and the low-byte register as DPL, which can be handled either as a single 16-bit register DPRT or as two independent 8-bit registers DPH and DPL. It contains dual data pointers (DPTR & DPTR1) that can be selected via the DPS (bit 0) register.

3 Memory

3.1 Main Features

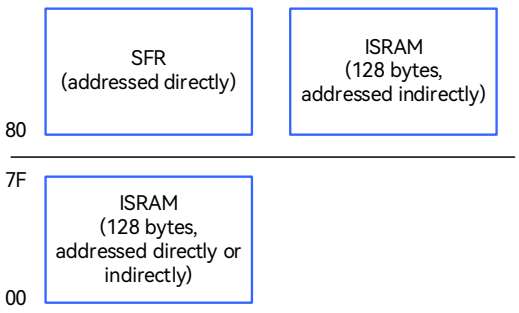
The memory consists of internal RAM (ISRAM) and external memory space, the latter of which contains the program memory EFLASH for storing user programs.

3.2 Internal RAM (ISRAM)

The chip provides 256 bytes of internal RAM (ISRAM) for data storage, accessible via the MOV instruction. ISRAM is divided into lower 128 bytes and upper 128 bytes.

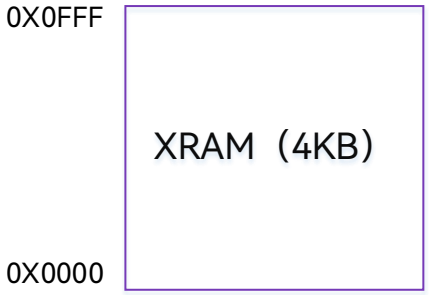
- The lower 128 bytes of ISRAM (addresses from 00H to 7FH) can be accessed directly or indirectly.
- The upper 128 bytes of ISRAM (addresses from 80H to FFH) can only be accessed indirectly.
- Special function register (SFR, addresses from 80H to FFH) can only be accessed directly.
- External RAM can be accessed directly via the MOVX instruction.

The upper 128 bytes of ISRAM occupy the same address space as the SFR, but are physically separated from the SFR space. When an instruction accesses an internal address higher than 7FH, the CPU can distinguish whether to access the upper 128 bytes of data ISRAM or the SFR based on the type of instruction being executed.



3.3 External Storage Memory

The chip provides 4K Bytes of external random access memory (XRAM) for data storage.



3.4 External Storage Memory Mapping

There are two boot modes for the chip: Boot mode and Main mode. The specific boot process is as follows:

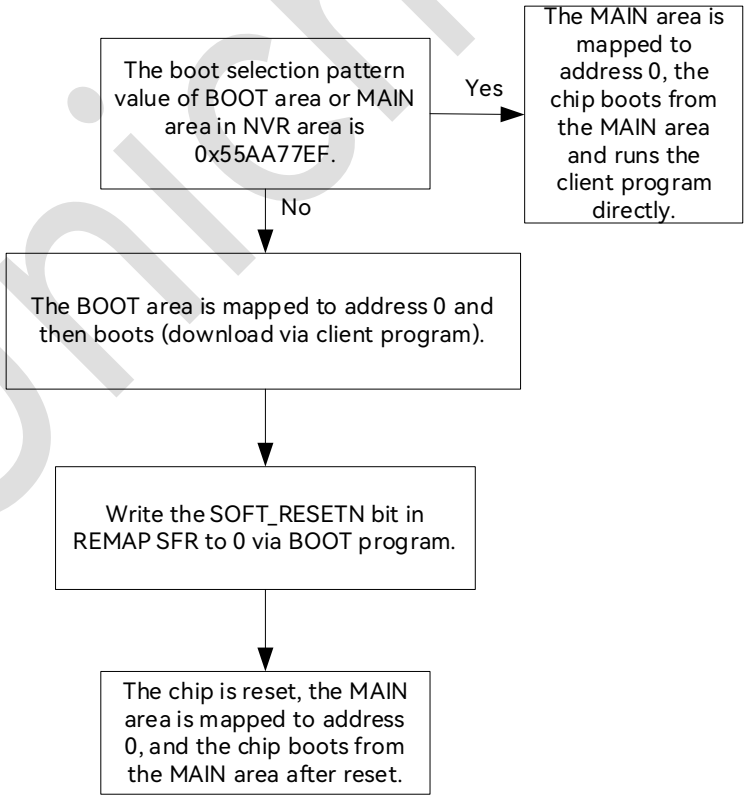
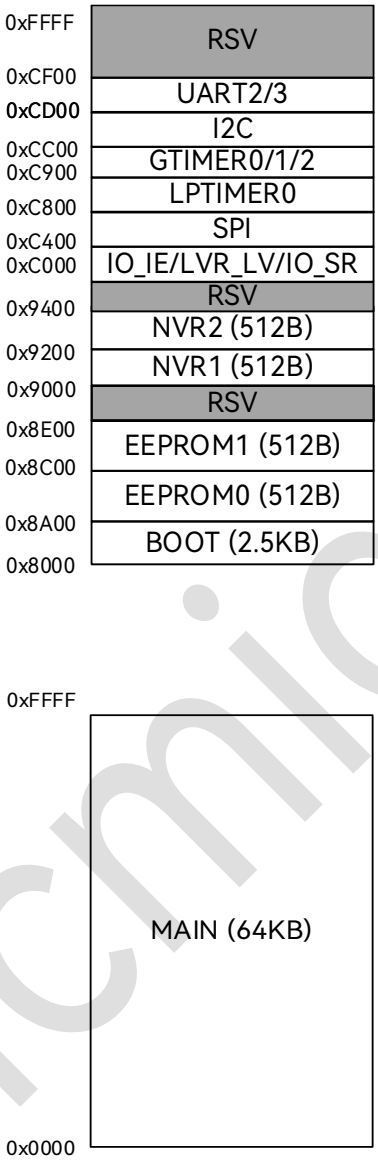


Figure 3-1: Chip Boot Flowchart

The address mapping after remapping is as follows:



Note:

- The BOOT area, NVR area, EEPROM0 area, and EEPROM1 area are accessed using the xdata keyword.
- Data in the SRAM area is accessed using the xdata keyword.
- The base address of the Main area is 0x0000, which is accessed using the code keyword.

3.5 Program Memory EFLASH

Main features of EFLASH:

- UM800YA includes 64K Bytes of program space.
- The EFLASH of UM800YA supports the IAP function (in-application programming).
- Data retention: at least 10 years

EFLASH programming (EFLASH can be read and written in the following two ways):

1. IAP mode, where user program code can program unused EFLASH areas. For details, please refer to the chapter of "EFC".
2. Through the system Boot program, EFLASH can be programmed via the serial port.

4 System Configuration (SFR)

4.1 Register Description

Table 4-1: List of Registers

Address	Name	Description
80H	P0	P0 Register
81H	SP	Stack pointer register
82H–85H	DPTR	Data pointer register
87H	PCON	PCON register
8EH	PDSEL	Power-down mode selection bit register
8FH	POREN	Power-down reset enable register
90H	P1	P1 Register
91H	LDOTRIML	Bandgap trimming register
92H	DPS	Data pointer selection register
97H	P0DR	Port P0 drive capability configuration register
9AH	IEN2	Interrupt enable register
BCH	RCLTRIML	On-chip low-frequency RCL trim value low-byte register
9FH	RCLTRIM	On-chip low-frequency RCL trim value high-byte register
A0H	P2	P2 Register
A1H	OUS	Flash erase/write time scale register
A4H	P0AL	P0_0–3 port interrupt rising/falling edge enable register
A8H	IEN0	Interrupt enable register
A9H	IP0	Interrupt priority register
B9H	IP1	Interrupt priority register
ABH	P0AH	P0_4 port interrupt rising/falling edge enable register
AEH	P1AL	P1_0–3 port interrupt rising/falling edge enable register
AFH	REMAP	REMAP register
B0H	P1AH	P1_4–5 port interrupt rising/falling edge enable register
B1H	CLKST	System clock setting register
B2H	ESTCR	External reset enable register
B3H	XTHCTR	External XTH clock register
B6H	ADCDR0	A/D channel received data low-byte register
B7H	ADCDR1	A/D channel received data high-byte register

Address	Name	Description
B8H	IEN1	Interrupt enable register
BDH	LDOTRIMH	Bandgap trimming register
BEH	RCHTRIMH	On-chip high-frequency RCH trim value high-byte register
BFH	RCHTRIML	On-chip high-frequency RCH trim value low-byte register
C0H	P2AL	P2_0–3 port interrupt rising/falling edge enable register
D0H	PSW	Program status word register
D5H	P0PD	Port P0 pull-down configuration register
D6H	P0OD	Port P0 open-drain output configuration register
D7H	P0CS	Port P0 input type configuration register
D9H	SYSDIV	High frequency clock (RC16M or XCLK) divider control register
DAH	P1PD	Port P1 pull-down configuration register
DBH	P1OD	Port P1 open-drain output configuration register
DCH	P1CS	Port P1 input type configuration register
DEH	PCLK0	Clock enable/disable register
DFH	PCLK1	Clock enable/disable register
E0H	ACC	Accumulator register
E1H–E3H	PxIRQ	Port interrupt flag register
E4H	P2PD	Port P2 pull-down configuration register
E5H	P1DR	Port P1 drive capability configuration register
E6H	PRESET0	Reset release register
E7H	PRESET1	Reset release register
P2AH	P2AH	P2_5–7 port interrupt rising/falling edge enable register
E9H–EBH	PxIEN	Port interrupt enable control register
ECH	P2OD	Port P2 open-drain output configuration register
F0H	B	B register
F1H–F3H	PxPUN	Port pull-up enable control register
F4H	P2CS	Port P2 input type configuration register
F8H	CLKCON	System clock register
F9H–FBH	PxOEN	Port direction control register
FCH	P2DR	Port P2 drive capability configuration register

4.1.1 P0

80H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0	-	-	-	P0.4	P0.3	P0.2	P0.1	P0.0
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	1	1	1

Bit No.	Bit Designator	Description
7:5	-	-
4	P0.4	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
3	P0.3	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
2	P0.2	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
1	P0.1	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
0	P0.0	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.

4.1.2 SP

81H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SP	SP							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1

Bit No.	Bit Designator	Description
7:0	SP	The stack pointer SP is an 8-bit dedicated register whose value can be updated via write operations. ● When executing instructions such as PUSH, various subroutine calls, and interrupt response, the SP is first incremented by 1, and then the data is pushed onto the stack. ● When executing instructions such as POP, RET, RETI, etc., the data is popped from the stack, and then the SP is decremented by 1. The top of the stack can be any address in the on-chip internal RAM (00H–FFH). After system reset, the SP is initialized to 07H, effectively starting the stack from address 08H.

4.1.3 DPTR

82H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DPL	DPL							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	DPL	Low 8 bits of the data pointer DPTR0

83H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DPH	DPH							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	DPH	High 8 bits of the data pointer DPTR0

4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DPL1	DPL1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	DPL1	Lower 8 bits of the data pointer DPTR1

85H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DPH1	DPH1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	DPH1	Higher 8 bits of the data pointer DPTR1

4.1.4 PCON

87H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCON	-	-	-	-	-	-	STOP	IDLE
R/W	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:2	-	-
1	STOP	Writing 1 enters the Stop mode, and reading always returns 0.
0	IDLE	Writing 1 enters the Idle mode, and reading always returns 0.

4.1.5 PDSEL

8EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PDSEL	-	-	-	-	-	-	-	PDSEL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:1	-	-
0	PDSEL	Power-down mode selection bit: ● 1: Power-down mode enabled. When this bit is 1, writing 1 to the STOP bit in PCON will enter Power-down mode, where all system clock sources are turned off. ● 0: Power-down mode disabled. When this bit is 1, writing 1 to the STOP bit in PCON will enter Stop mode, where the system RCL remains running, while the XTH and RCH are turned off.

4.1.6 POREN

8FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
POREN	-							LVR_ENB
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0

Bit No.	Bit Designator	Description
7:1	-	-
0	LVR_ENB	Power-down reset enable bit: 0: Power-down reset enabled 1: Power-down reset disabled

4.1.7 P1

90H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1	-	-	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0
R/W	-	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	-	-	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7:6	-	-
5	P1.5	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
4	P1.4	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
3	P1.3	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
2	P1.2	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.
1	P1.1	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.

0	P1.0	● When the port is configured as output state: 0: Output low level 1: Output high level ● When the port is configured as input state: The value read is the port status.

4.1.8 LDOTRIML

91H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDOTRIML	-			VTRM_BGRVT				
R/W	R			R/W				
Reset Value	0			5'h0F				

Bit No.	Bit Designator	Description
7:5	-	-
4:0	VTRM_BGRVT	Bandgap trim bits

4.1.9 DPS

92H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DPS	-	-	-	-	-	-	-	DPS
R/W	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:1	-	-
0	DPS	1: Select DPTR1 as data pointer. 0: Select DPTR0 as data pointer.

4.1.10 P0DR

97H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0DR	-	-	-	P0_4DR	P0_3DR	P0_2DR	P0_1DR	P0_0DR
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:5	-	-
4	P0_4DR	Port P0_4 drive capability configuration register: 0: High drive capability 1: Low drive capability
3	P0_3DR	Port P0_3 drive capability configuration register: 0: High drive capability 1: Low drive capability
2	P0_2DR	Port P0_2 drive capability configuration register: 0: High drive capability 1: Low drive capability
1	P0_1DR	Port P0_1 drive capability configuration register: 0: High drive capability 1: Low drive capability
0	P0_0DR	Port P0_0 drive capability configuration register: 0: High drive capability 1: Low drive capability

4.1.11 IEN2

9AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN2	-	-	-	-	-	-	-	UART3INTEN
R/W	R	-	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:1	-	-
0	UART3INTEN	UART3 interrupt enable: 1: Enabled 0: Disabled

4.1.12 RCLTRIML

BCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCLTRIML	RCLTCTRIM				-			RCLTRIML
R/W	R/W				R			R/W

Reset Value	0x7	0	0x1

Bit No.	Bit Designator	Description
7:4	RCLTCTRIM	On-chip RCL temperature drift trimming value
3:1	-	-
0	RCLTRIML	On-chip RCL trimming value low-order bit

4.1.13 RCLTRIM

9FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCLTRIM	RCLTRIMH							
R/W	R/W							
Reset Value	0x7F							

Bit No.	Bit Designator	Description
7:0	RCLTRIMH	On-chip RCL trimming value high-order bit

4.1.14 P2

A0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2	P2.7	P2.6	P2.5	-	P2.3	P2.2	-	P2.0
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	1	1	1	0	1	1	0	1

Bit No.	Bit Designator	Description
7	P2.7	**When the port is configured as output state:** 0: Output low level 1: Output high level **When the port is configured as input state:** The value read is the port status.
6	P2.6	**When the port is configured as output state:** 0: Output low level 1: Output high level **When the port is configured as input state:** The value read is the port status.
5	P2.5	**When the port is configured as output state:**

		0: Output low level 1: Output high level **When the port is configured as input state:** The value read is the port status.
4	-	-
3	P2.3	**When the port is configured as output state:** 0: Output low level 1: Output high level **When the port is configured as input state:** The value read is the port status
2	P2.2	**When the port is configured as output state:** 0: Output low level 1: Output high level **When the port is configured as input state:** The value read is the port status.
1	-	-
0	P2.0	**When the port is configured as output state:** 0: Output low level 1: Output high level **When the port is configured as input state:** The value read is the port status.

4.1.15 OUS

A1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OUS	-	-	-	OUS				
R/W	-	-	-	R/W	R/W	R/W	R/W	R/W
Reset Value	-	-	-	0	0	1	1	1

Bit No.	**Bit Designator**	**Description**
7:5	-	-
4:0	OUS	Flash erase/write time scale The default value of this register is 0xF, which is set according to NVR table in actual application.

4.1.16 P0AL

A4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0AL	P0AL.7	P0AL.6	P0AL.5	P0AL.4	P0AL.3	P0AL.2	P0AL.1	P0AL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7	P0AL.7	Port P0_3 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
6	P0AL.6	Port P0_3 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
5	P0AL.5	Port P0_2 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
4	P0AL.4	Port P0_2 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
3	P0AL.3	Port P0_1 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
2	P0AL.2	Port P0_1 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
1	P0AL.1	Port P0_0 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
0	P0AL.0	Port P0_0 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge

4.1.17 IEN0

A8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN0	EA	EADC	EPWM	ES0	-	ES1	-	EX0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	EA	Global interrupt enable: 0: Disable the interrupt. 1: Enable the interrupt.
6	EADC	ADC interrupt enable: 0: Disable the interrupt. 1: Enable the interrupt.
5	EPWM	PWM interrupt enable: 0: disabled 1: enabled
4	ES0	UART0 interrupt enable: 0: Disable the interrupt. 1: Enable the interrupt.
3	-	-
2	ES1	UART1 interrupt enable: 0: Disable the interrupt. 1: Enable the interrupt.
1	-	-
0	EX0	External interrupt primary enable: 0: Disable the interrupt. 1: Enable the interrupt.

4.1.18 IP

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IP0 (A9H)	-	-	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0
IP1 (B9H)	-	-	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Each interrupt source can be individually set to one of the four interrupt priorities, which is achieved by configuring the corresponding bits of IP0 and IP1, as detailed in the following table:

IP1.x	IP0.x	Priority Level
0	0	Level 0 (lowest)
0	1	Level 1
1	0	Level 2
1	1	Level 3 (highest)

Bit	Corresponding Interrupts
IP1.0, IP0.0	External interrupt 0 (EX0), ADC interrupt, and UART2 interrupt
IP1.1, IP0.1	SPI interrupt, UART3 interrupt
IP1.2, IP0.2	UART1 interrupt (ES1)
IP1.3, IP0.3	GTIMER2 interrupt, EFC interrupt
IP1.4, IP0.4	UART0 interrupt (ES0), GTIMER1 interrupt and LPTIMER interrupt
IP1.5, IP0.5	PWM interrupt (EPWM), GTIMER0 interrupt and I2C interrupt

4.1.19 P0AH

ABH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0AH	-	-	-	-	-	-	P0AH.1	P0AH.0
R/W	R	R	R	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1

Bit No.	Bit Designator	Description
7:2	-	-
1	P0AH.1	Port P0_4 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
0	P0AH.0	Port P0_4 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge

4.1.20 P1AL

AEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1AL	P1AL.7	P1AL.6	P1AL.5	P1AL.4	P1AL.3	P1AL.2	P1AL.1	P1AL.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7	P1AL.07	Port P1_3 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
6	P1AL.06	Port P1_3 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
5	P1AL.05	Port P1_2 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
4	P1AL.04	Port P1_2 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
3	P1AL.3	Port P1_1 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
2	P1AL.2	Port P1_1 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
1	P1AL.1	Port P1_0 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
0	P1AL.0	Port P1_0 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge

4.1.21 REMAP

AFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
REMAP	-	-	-	-	-	REMAP_FLAG	REMAP_IM	REMAP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1

Bit No.	Bit Designator	Description
7:3	-	-
2	REMAP_FLAG	Flag indicating whether the system has undergone remapping: 1: The system has undergone remapping. 0: The system has not undergone remapping.
1	REMAP_IM	0: The address is directly remapped.
0	REMAP	0: The address is remapped, and a system reset is generated; after reset, the system boots from the main area of eFlash.

4.1.22 P1AH

B0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1AH	-	-	-	-	P1AH.3	P1AH.2	P1AH.1	P1AH.0
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	1	1	1	1

Bit No.	Bit Designator	Description
7:4	-	-
3	P1AH.3	Port P1_5 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
2	P1AH.2	Port P1_5 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
1	P1AH.1	Port P1_4 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge

0	P1AH.0	Port P1_4 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge

4.1.23 CLKST

B1H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKST	WACKDELAY		XTHSTAB		RCHSTAB		RCLSTAB	
RW	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	1	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	WACKDELAY	Wake-up delay setting: 00: 64 system clock cycles 01: 128 system clock cycles 10: 161 system clock cycles 11: 184 system clock cycles
5:4	XTHSTAB	XTH stabilization time setting: 00: 1024 XTH clock cycles 01: 4096 XTH clock cycles 10: 16384 XTH clock cycles 11: 32768 XTH clock cycles
3:2	RCHSTAB	RCH stabilization time setting: 00: 1 RCH16M clock cycles 01: 4 RCH16M clock cycles 10: 32 RCH16M clock cycles 11: 256 RCH16M clock cycles
1:0	RCLSTAB	RCL stabilization time setting: 00: 1 RCL38K clock cycles 01: 4 RCL38K clock cycles 10: 32 RCL38K clock cycles 11: 256 RCL38K clock cycles

4.1.24 ESTCR

B2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ESTCR	-	-	-	-	ERSTEN	-	-	ERSTLVEN
R/W	R	R	R	R	R/W	R	R	R/W
Reset Value	0	0	0	0	1	0	0	0

Bit No.	Bit Designator	Description
7:4	-	-
3	ERSTEN	External reset pin enable bit: 1: External reset function enabled 0: External reset function disabled
2:1	-	-
0	ERSTLVEN	1: External reset filter enabled 0: External reset filter disabled

4.1.25 XTHCTR

B3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
XTHCTR	-	-	-	-	EXTH_GSEL			EXTH_EN
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	0

Bit No.	Bit Designator	Description
7:4	-	-
3:1	EXTH_GSEL	XTH trim bits
0	EXTH_EN	External XTH clock input control: 1: XTH clock is input from P0_0. 0: XTH clock is generated by the crystal oscillator. Note: When using P0_0 for clock input, XCLKEN must be set to 1.

Crystal Frequency	GSEL[2:0>	RSEL[1:0]
F ≤ 1 MHz	000	00
1 MHz < F ≤ 6 MHz	001	01
6 MHz < F ≤ 12 MHz	010	10
12 MHz < F ≤ 16 MHz	011	10

4.1.26 ADCDR0

B6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCDR0	CHDATAL							
R/W	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	CHDATAL	A/D channel received data low-byte register

4.1.27 ADCDR1

B7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADCDR1	-	-	-	-	CHDATAH			
R/W	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	-	-
6:4	-	-
3:0	CHDATAH	A/D channel received data high-byte register

4.1.28 IEN1

B8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IEN1	UART2INTEN	GTIMER2INTEN	I2CINTEN	LPTIMERINTEN	EFCINTEN	GTIMER1INTEN	SPIINTEN	GTIMER0INTEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	UART2INTEN	UART2 interrupt enable: 1: Enabled; 0: Disabled
6	GTIMER2INTEN	GTIMER2 interrupt enable: 1: Enabled; 0: Disabled

5	I2CINTEN	I2C interrupt enable: 1: Enabled; 0: Disabled
4	LPTIMERINTEN	LPTIMER interrupt enable: 1: Enabled; 0: Disabled
3	EFCINTEN	EFC interrupt enable: 1: Enabled; 0: Disabled
2	GTIMER1INTEN	GTIMER1 interrupt enable: 1: Enabled; 0: Disabled
1	SPIINTEN	SPI interrupt enable: 1: Enabled; 0: Disabled
0	GTIMER0INTEN	GTIMER0 interrupt enable: 1: Enabled; 0: Disabled

4.1.29 LDOTRIMH

BDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LDOTRIMH	-			VTRM_BGRTT				
R/W	R			R/W				
Reset Value	0			5'h0				

Bit No.	Bit Designator	Description
7:5	-	-
4:0	VTRM_BGRTT	Bandgap trim bits

4.1.30 RCHTRIMH

BEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCHTRIMH	RCHTRIMH							
R/W	R/W							
Reset Value	0x0							

Bit No.	Bit Designator	Description
7:0	RCHTRIMH	On-chip high-frequency RCH fine-tunning value

4.1.31 RCHTRIML

BFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
RCHTRIML	RCHCTRIM				-	-	-	-
R/W	R/W				R	R	R	R
Reset Value	0x3				0	0	0	0

Bit No.	Bit Designator	Description
7:4	RCHCTRIM	On-chip high-frequency RCH coarse-tunning value
3:0	-	-

4.1.32 P2AL

C0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2AL	P2AL.7	P2AL.6	P2AL.5	P2AL.4	-	-	P2AL.1	P2AL.0
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Reset Value	1	1	1	1	0	0	1	1

Bit No.	Bit Designator	Description
7	P2AL.7	Port P2_3 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
6	P2AL.6	Port P2_3 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
5	P2AL.5	Port P2_2 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
4	P2AL.4	Port P2_2 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
3:2	-	-
1	P2AL.1	Port P2_0 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge

0	P2AL.0	Port P2_0 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge

4.1.33 PSW

D0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSW	CY	AC	F0	RS1	RS0	OV	F1	P
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	CY	Carry flag: This bit is set to 1 when the last arithmetic operation generates a carry (in addition) or a borrow (in subtraction), and it is cleared to 0 by other arithmetic operations.
6	AC	Auxiliary carry flag: This bit is set to 1 when the last arithmetic operation generates a carry (in addition) to or a borrow (in subtraction) from the high nibble, and it is cleared to 0 by other arithmetic operations.
5	F0	User flag 0: This is a bit-addressable general-purpose flag bit for software control.
4:3	RS[1:0]	RS1:RS0: register bank selection: 00: Bank 0 (mapped to 00H–07H) 01: Bank 1 (mapped to 08H–0FH) 10: Bank 2 (mapped to 10H–17H) 11: Bank 3 (mapped to 18H–1FH)
1	F1	User flag 1: This is a bit-addressable general-purpose flag bit for software control.
0	P	Parity bit: 0: The sum of the 8 bits in the accumulator is even. 1: The sum of the 8 bits in the accumulator is odd.

4.1.34 P0PD

D5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PD	-	-	-	P0_4PD	P0_3PD	P0_2PD	P0_1PD	P0_0PD
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:5	-	-
4	P0_4PD	Port P0_4 pull-down configuration register: 0: Disabled 1: Enabled
3	P0_3PD	Port P0_3 pull-down configuration register: 0: Disabled 1: Enabled
2	P0_2PD	Port P0_2 pull-down configuration register: 0: Disabled 1: Enabled
1	P0_1PD	Port P0_1 pull-down configuration register: 0: Disabled 1: Enabled
0	P0_0PD	Port P0_0 pull-down configuration register: 0: Disabled 1: Enabled

4.1.35 P0OD

D6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0OD	-	-	-	P0_4OD	P0_3OD	P0_2OD	P0_1OD	P0_0OD
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:5	-	-

4	P0_4OD	Port P0_4 open-drain output configuration register: 0: Disabled 1: Enabled
3	P0_3OD	Port P0_3 open-drain output configuration register: 0: Disabled 1: Enabled
2	P0_2OD	Port P0_2 open-drain output configuration register: 0: Disabled 1: Enabled
1	P0_1OD	Port P0_1 open-drain output configuration register: 0: Disabled 1: Enabled
0	P0_0OD	Port P0_0 open-drain output configuration register: 0: Disabled 1: Enabled

4.1.36 P0CS

D7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0CS	-	-	-	P0_4CS	P0_3CS	P0_2CS	P0_1CS	P0_0CS
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:5	-	-
4	P0_4CS	Port P0_4 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
3	P0_3CS	Port P0_3 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
2	P0_2CS	Port P0_2 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
1	P0_1CS	Port P0_1 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer

0	P0_0CS	Port P0_0 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer

4.1.37 SYSDIV

D9H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SYSDIV	-	-	-	-	-	SYSDIV[2]	SYSDIV[1]	SYSDIV[0]
R/W	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0

Bit No.	Bit Designator	Description
7:3	-	-
2:0	SYSDIV[1:0]	Frequency division control of high-frequency clock (RC16M or XCLK), with the divided output serving as the system clock: 000: HSCLK is not divided. 001: HSCLK is divided by 2. 010: HSCLK is divided by 4. 011: HSCLK is divided by 8. 100: HSCLK is divided by 16. 101: HSCLK is divided by 32. 110: HSCLK is divided by 64. 111: HSCLK is divided by 128.

4.1.38 P1PD

DAH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1PD	-	-	P1_5PD	P1_4PD	P1_3PD	P1_2PD	P1_1PD	P1_0PD
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	-	-
5	P1_5PD	Port P1_5 pull-down configuration register: 0: Disabled 1: Enabled
4	P1_4PD	Port P1_4 pull-down configuration register:

		0: Disabled 1: Enabled
3	P1_3PD	Port P1_3 pull-down configuration register: 0: Disabled 1: Enabled
2	P1_2PD	Port P1_2 pull-down configuration register: 0: Disabled 1: Enabled
1	P1_1PD	Port P1_1 pull-down configuration register: 0: Disabled 1: Enabled
0	P1_0PD	Port P1_0 pull-down configuration register: 0: Disabled 1: Enabled

4.1.39 P1OD

DBH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1OD	-	-	P1_5OD	P1_4OD	P1_3OD	P1_2OD	P1_1OD	P1_0OD
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	-	-
5	P1_5OD	Port P1_5 open-drain output configuration register: 0: Disabled 1: Enabled
4	P1_4OD	Port P1_4 open-drain output configuration register: 0: Disabled 1: Enabled
3	P1_3OD	Port P1_3 open-drain output configuration register: 0: Disabled 1: Enabled
2	P1_2OD	Port P1_2 open-drain output configuration register: 0: Disabled 1: Enabled
1	P1_1OD	Port P1_1 open-drain output configuration register:

		0: Disabled 1: Enabled
0	P1_0OD	Port P1_O open-drain output configuration register: 0: Disabled 1: Enabled

4.1.40 P1CS

DCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1CS	-	-	P1_5CS	P1_4CS	P1_3CS	P1_2CS	P1_1CS	P1_0CS
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	-	-
5	P1_5CS	Port P1_5 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
4	P1_4CS	Port P1_4 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
3	P1_3CS	Port P1_3 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
2	P1_2CS	Port P1_2 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
1	P1_1CS	Port P1_1 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
0	P1_0CS	Port P1_0 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer

4.1.41 PCLK0

DEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCLK0	I2CCEN	LPTIMCEN	PWMCEN	ADCCEN	SPICEN	WDTCEN	UART1CEN	UART0CEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7	I2CCEN	1: I2C clock enabled 0: I2C clock disabled
6	LPTIMCEN	1: LPTIMER clock enabled 0: LPTIMER clock disabled
5	PWMCEN	1: PWM clock enabled 0: PWM clock disabled
4	ADCCEN	1: ADC enabled 0: ADC clock disabled
3	SPICEN	1: SPI enabled 0: SPI clock disabled
2	WDTCEN	1: WDT clock enabled 0: WDT clock disabled
1	UART1CEN	1: UART1 clock enabled 0: UART1 clock disabled
0	UART0CEN	1: UART0 enabled 0: UART0 clock disabled

4.1.42 PCLK1

DFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PCLK1	UART2CEN	GTIMER2CEN	GTIMER1CEN	-	GTIMER0CEN	GIO2CEN	GIO1CEN	GIO0CEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7	UART2CEN	1: UART2 enabled 0: UART2 clock disabled
6	GTIMER2CEN	1: GTIMER2 clock enabled 0: GTIMER2 clock disabled
5	GTIMER1CEN	1: GTIMER1 clock enabled 0: GTIMER1 clock disabled
4	-	-
3	GTIMER0CEN	1: GTIMER0 enabled 0: GTIMER0 clock disabled
2	GIO2CEN	1: GPIO2 enabled 0: GPIO2 clock disabled
1	GIO1CEN	1: GPIO1 clock enabled 0: GPIO1 clock disabled
0	GIO0CEN	1: GPIO0 clock enabled 0: GPIO0 clock disabled

4.1.43 ACC

E0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ACC	ACC							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	ACC	The accumulator ACC is a commonly used dedicated register used to store the operands involved in operations and the operation results.

4.1.44 PxIRQ

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0IRQ (E1H)	-	-	-	P0IRQ.4	P0IRQ.3	P0IRQ.2	P0IRQ.1	P0IRQ.0

P1IRQ (E2H)	-	-	P1IRQ.5	P1IRQ.4	P1IRQ.3	P1IRQ.2	P1IRQ.1	P1IRQ.0
P2IRQ (E3H)	P2IRQ.7	P2IRQ.6	P2IRQ.5	-	P2IRQ.3	P2IRQ.2	-	P2IRQ.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	PxIRQ.y x = 0-4, y = 0-7	Port interrupt flag bit: 0: No interrupt is generated by the port. 1: An interrupt is generated by the port. Writing 0 clears the bit.

4.1.45 P2PD

E4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2PD	P2_7PD	P2_6PD	P2_5PD	-	P2_3PD	P2_2PD	-	P2_0PD
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	P2_7PD	Port P2_7 pull-down configuration register: 0: Disabled 1: Enabled
6	P2_6PD	Port P2_6 pull-down configuration register: 0: Disabled 1: Enabled
5	P2_5PD	Port P2_5 pull-down configuration register: 0: Disabled 1: Enabled
4	-	-
3	P2_3PD	Port P2_3 pull-down configuration register: 0: Disabled 1: Enabled
2	P2_2PD	Port P2_2 pull-down configuration register: 0: Disabled

		1: Enabled
1	-	-
0	P2_0PD	Port P1_0 pull-down configuration register: 0: Disabled 1: Enabled

4.1.46 P1DR

E5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1DR	-	-	P1_5DR	P1_4DR	P1_3DR	P1_2DR	P1_1DR	P1_0DR
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7:6	-	-
5	P1_5DR	Port P1_5 drive capability configuration register: 0: High drive capability 1: Low drive capability
4	P1_4DR	Port P1_4 drive capability configuration register: 0: High drive capability 1: Low drive capability
3	P1_3DR	Port P1_3 drive capability configuration register: 0: High drive capability 1: Low drive capability
2	P1_2DR	Port P1_2 drive capability configuration register: 0: High drive capability 1: Low drive capability
1	P1_1DR	Port P1_1 drive capability configuration register: 0: High drive capability 1: Low drive capability
0	P1_0DR	Port P1_0 drive capability configuration register: 0: High drive capability 1: Low drive capability

4.1.47 PRESET0

E6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PRESET0	I2CREN	LPTIMREN	PWMREN	ADCREN	SPIREN	WDTREN	UART1REN	UART0REN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7	I2CREN	1: I2C reset released 0: I2C reset
6	LPTIMREN	1: LPTIMER reset released 0: LPTIMER reset
5	PWMREN	1: PWM reset released 0: PWM reset
4	ADCREN	1: ADC reset released 0: ADC reset
3	SPIREN	1: SPI reset released 0: SPI reset
2	WDTREN	1: WDT reset released 0: WDT reset
1	UART1REN	1: UART1 reset released 0: UART1 reset
0	UART0REN	1: UART0 reset released 0: UART0 reset

4.1.48 PRESET1

E7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PRESET1	UART2REN	GTIMER2REN	GTIMER1REN	-	GTIMER0REN	GIO2REN	GIO1REN	GIO0REN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7	UART2REN	1: UART2 reset released 0: UART2 reset
6	GTIMER2REN	1: GTIMER2 reset released 0: GTIMER2 reset
5	GTIMER1REN	1: GTIMER1 reset released 0: GTIMER1 reset
4	-	-
3	GTIMER0REN	1: GTIMER0 reset released 0: GTIMER0 reset
2	GIO2REN	1: GPIO2 reset released 0: GPIO2 reset
1	GIO1REN	1: GPIO1 reset released 0: GPIO1 reset
0	GIO0REN	1: GPIO0 reset released 0: GPIO0 reset

4.1.49 P2AH

E8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2AH	P2AH.7	P2AH.6	P2AH.5	P2AH.4	P2AH.1	P2AH.0	-	-
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R
Reset Value	1	1	1	1	1	1	0	0

Bit No.	Bit Designator	Description
7	P2AH.7	Port P2_7 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
6	P2AH.6	Port P2_7 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
5	P2AH.5	Port P2_6 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
4	P2AH.4	Port P2_6 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge

		1: Enable port interrupt triggered by rising edge
3	P2AH.1	Port P2_5 falling-edge triggered interrupt enable bit: 0: Disable port interrupt triggered by falling edge 1: Enable port interrupt triggered by falling edge
2	P2AH.0	Port P2_5 rising-edge triggered interrupt enable bit: 1: Disable port interrupt triggered by rising edge 1: Enable port interrupt triggered by rising edge
1:0	-	-

4.1.50 PxIEN

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0IEN (E9H)	-	-	-	P0IEN.4	P0IEN.3	P0IEN.2	P0IEN.1	P0IEN.0
P1IEN (EAH)	-	-	P1IEN.5	P1IEN.4	P1IEN.3	P1IEN.2	P1IEN.1	P1IEN.0
P2IEN (EBH)	P2IEN.7	P2IEN.6	P2IEN.5	-	P2IEN.3	P2IEN.2	-	P2IEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	PxIEN.y x = 0-4, y = 0-7	Port interrupt enable bit: 0: Disable the interrupt. 1: Enable the interrupt.

4.1.51 P2OD

ECH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2OD	P2_7OD	P2_6OD	P2_5OD	-	P2_3OD	P2_2OD	-	P2_0OD
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	P2_7OD	Port P2_7 open-drain output configuration register: 0: Disabled 1: Enabled
6	P2_6OD	Port P2_6 open-drain output configuration register: 0: Disabled 1: Enabled

5	P2_5OD	Port P2_5 open-drain output configuration register: 0: Disabled 1: Enabled
4	-	-
3	P2_3OD	Port P2_3 open-drain output configuration register: 0: Disabled 1: Enabled
2	P2_2OD	Port P2_2 open-drain output configuration register: 0: Disabled 1: Enabled
1	-	-
0	P2_0OD	Port P2_0 open-drain output configuration register: 0: Disabled 1: Enabled

4.1.52 B

F0H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
B	B							
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	B	The B register is used in multiplication and division instructions, or function as a general-purpose temporary register in other instructions.

4.1.53 PxPUN

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0PUN (F1H)	-	-	-	P0PUN.4	P0PUN.3	P0PUN.2	P0PUN.1	P0PUN.0
P1PUN (F2H)	-	-	P1PUN.5	P1PUN.4	P1PUN.3	P1PUN.2	P1PUN.1	P1PUN.0

P2PUN (F3H)	P2PUN.7	P2PUN.6	P2PUN.5	-	P2PUN.3	P2PUN.2	-	P2PUN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7:0	PxPUN.y x = 0-4, y = 0-7	Port pull-up enable bit (pull-up resistor reference value: 60 kΩ): 0: Enable the internal pull-up resistor. 1: Disable the internal pull-up resistor.

4.1.54 P2CS

F4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2CS	P2_7CS	P2_6CS	P2_5CS	-	P2_3CS	P2_2CS	-	P2_0CS
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	P2_7CS	Port P2_7 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
6	P2_6CS	Port P2_6 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
5	P2_5CS	Port P2_5 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
4	-	-
3	P2_3CS	Port P2_3 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
2	P2_2CS	Port P2_2 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer
1	-	-

0	P2_0CS	Port P2_0 input type configuration register: 0: Schmitt input buffer 1: CMOS input buffer

4.1.55 CLKCON

F8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
CLKCON	SYSCLKSEL	RC38KF	RC16MF	XCLKF	RC38KEN	RC16MEN	XCLKEN	HSCLKSEL
R/W	R/W	R	R	R	R/W	R/W	R/W	R/W
Reset Value	0	1	1	0	1	1	0	0

Bit No.	Bit Designator	Description
7	SYSCLKSEL	System clock source selection bit (selects whether SYSCLK is derived from HSCLK or RCL38K): 0: Select HSCLK as the system clock source. 1: Select RCL38K as the system clock source.
6	RC38KF	RC38K clock source status flag: 0: RC38K is not properly started. 1: RC38K is properly started.
5	RC16MF	RC16M clock source status flag: 0: RC16M is not properly started. 1: RC16M is properly started.
4	XCLKF	XCLK clock source status flag: 0: No valid external input clock is detected. 1: A valid external input clock is detected.
3	RC38KEN	RC38K clock source enable bit: 0: Disable RC38K. 1: Enable RC38K.
2	RC16MEN	RC16M clock source enable bit: 0: Disable the internal RC16M clock source. Writing 0 is invalid if the current system clock is RC16M. 1: Enable the internal RC16M clock source.
1	XCLKEN	XCLK clock source enable bit: 0: Disable XCLK. P0.0 and P0.1 function as GPIOs. If the current system clock is XCLK, writing 0 to XCLKEN will not disable XCLK.

		1: Enable XCLK. P0.0 and P0.1 function as crystal or external clock input.
0	HSCLKSEL	High-frequency clock source selection bit (selects whether HSCLK is derived from RCH16M and XCLK): 0: Select RC16M as the system clock source. 1: Select XCLK as the system clock source.

4.1.56 PxOEN

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0OEN (F9H)	-	-	-	P0OEN.4	P0OEN.3	P0OEN.2	P0OEN.1	P0OEN.0
P1OEN (FAH)	-	-	P1OEN.5	P1OEN.4	P1OEN.3	P1OEN.2	P1OEN.1	P1OEN.0
P2OEN (FBH)	P2OEN.7	P2OEN.6	P2OEN.5	-	P2OEN.3	P2OEN.2	-	P2OEN.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7:0	PxOEN.y x = 0-4, y = 0-7	Port direction control bit: 0: Output mode 1: Input mode

4.1.57 P2DR

FCH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2DR	P2_7DR	P2_6DR	P2_5DR	-	P2_3DR	P2_2DR	-	P2_0DR
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	1	1	1	0	1	1	0	1

Bit No.	Bit Designator	Description
7	P2_7DR	Port P2_7 drive capability configuration register: 0: High drive capability 1: Low drive capability
6	P2_6DR	Port P2_6 drive capability configuration register:

		0: High drive capability 1: Low drive capability
5	P2_5DR	Port P2_5 drive capability configuration register: 0: High drive capability 1: Low drive capability
4	-	-
3	P2_3DR	Port P2_3 drive capability configuration register: 0: High drive capability 1: Low drive capability
2	P2_2DR	Port P2_2 drive capability configuration register: 0: High drive capability 1: Low drive capability
1	-	-
0	P2_0DR	Port P2_0 drive capability configuration register: 0: High drive capability 1: Low drive capability

4.2 System Clock

4.2.1 Main Features

- Built-in 16MHz RC high-frequency oscillator
- Built-in 38kHz RC low-frequency oscillator
- Supporting external crystal oscillator input (2 MHz to 16 MHz) as the system clock.
- Built-in system clock divider

4.2.2 Clock Definitions

- RCH16M: the internal 16MHz RC high-frequency oscillator
- RCL38k: the internal 38kHz RC low-frequency oscillator
- XCLK: Crystal resonator clock (2 MHz–16 MHz crystal resonator) or external clock input

4.2.3 Clock Architecture Diagram

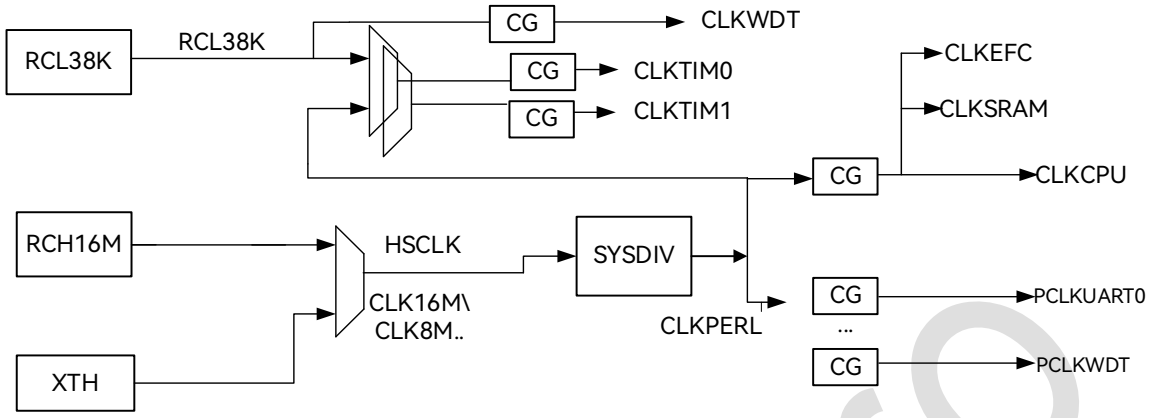


Figure 4-1: Clock Architecture Diagram

4.3 Reset Source

4.3.1 Main Features

Reset sources include:

- Pin reset
- LVD reset
- LVR
- WDT reset
- Power-on reset (POR)

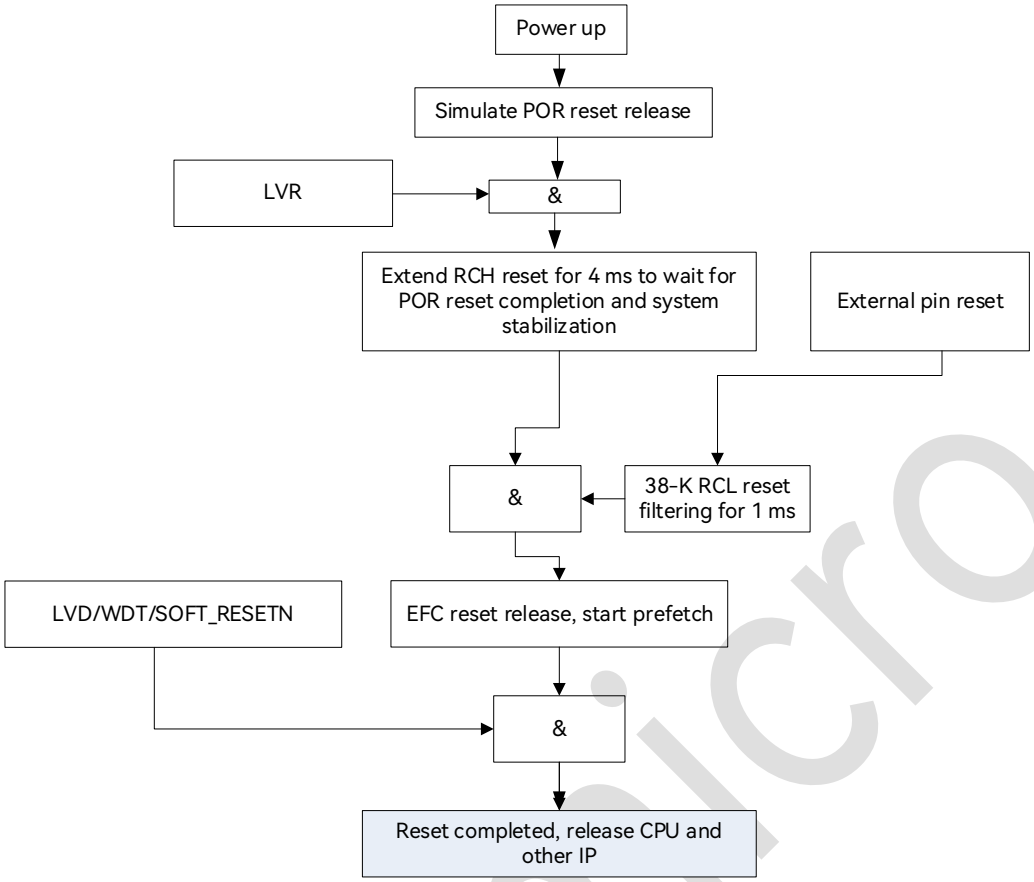


Figure 4-2: Reset Flow Chart

Note:

- When LVD reset occurs, the LVDCON register will not be reset.
- Both LVR and POR are global resets that reset all digital logic.

4.3.2 Watchdog Reset

The watchdog timer is an up-counter with the internal RC38K as its clock source. To enable the watchdog, the RC38K must be enabled first. In power-down mode, the watchdog will reset the chip when the timer overflows.

Reading or writing the RSTSTAT register automatically clears the watchdog counter.

4.3.3 LVD and LVR Resets

LVD is a low-voltage detection unit configurable via software to generate a reset when the

external supply voltage drops below the detection threshold. The LVD reset can reset the CPU and all peripherals except EFC.

LVR is a low-voltage reset unit with the same scope as POR, acting as a global reset. It can reset the entire chip when the external supply voltage falls below the fixed voltage of LVR (2.2 V).

4.3.4 External Reset

The external reset is a global reset with the same scope as POR. When RESETN IO is 0 and RESETN is used for external reset, the external reset is effective and the entire chip is reset.

4.3.5 Registers

For registers related to reset, please refer to the sections on POREN, LVD_RSTSTAT and LVD_CON.

4.4 Low-power Mode

4.4.1 Main Features

- Supporting three low-power modes: Sleep mode, DeepSleep mode and Stop mode
- All three low-power modes can be exited via interrupts or resets

4.4.2 Low-power Mode

In addition to the normal operating mode, the chip provides three low-power modes to reduce current consumption: Sleep mode, Deepsleep mode and Stop mode.

In Sleep mode, the CPU stops working while retaining the interrupt handling function. Clocks and resets for other peripherals and modules can be configured via software. Sleep mode is entered by writing 1 to a specific bit in the SFR (PCON -> IDLE) via software, and wake-up is

triggered by interrupts.

Deepsleep mode is an enhanced version of Sleep mode. In this mode, the CPU stops operating, the high-speed clock is disabled, while the low-power functional modules (LPTIMER and WDT) remain running. DeepSleep mode is entered by writing 1 to a specific bit in the SFR (PCON -> STOP) via software, and wake-up is triggered by interrupts.

In Stop mode, both the high-speed clock and the low-speed clock stop running, there are no running clocks in the system, and all peripheral modules stop operating. The power-on reset signal remains valid, IO states are retained, IO interrupts are enabled, and all registers, RAM and CPU data are preserved with minimal power consumption. To enter Stop mode, first set the PDSEL register in the SFR to 1, then write 1 to PCON -> STOP. Wake-up from Stop mode can only be initiated by the level change of an external pin.

4.4.3 Low-power Mode Table

Mode	Mode Description	Entry Condition	Exit Condition
Sleep	The CPU is mostly in sleep mode, software can disable the clocks of various modules.	1. Disable clocks of peripheral modules as needed, leaving only those required to monitor interrupt events. 2. Write 1 to PCON -> IDLE.	1. CPU detects an interrupt or event. 2. Enter the interrupt service routine to clear the interrupt and return. 3. Continue executing subsequent instructions.
Deep Sleep	The CPU is mostly in sleep mode, the high-speed clock source is disabled, and the low-speed clock source remains active.	1. Disable clocks of peripheral modules as needed, leaving only those required to monitor interrupt events. 2. Write 1 to PCON -> STOP.	1. CPU detects an interrupt or event. 2. Enter the interrupt service routine to clear the interrupt and return. 3. Continue executing subsequent instructions.

Mode	Mode Description	Entry Condition	Exit Condition
Stop	All system clocks are disabled.	1. Set the conditions for IO wake-up as required. 2. Set the PDSEL register in SFR to 1. 3. Write 1 to PCON -> STOP.	1. An external IO wake-up event occurs. 2. CPU detects an IO wake-up interrupt. 3. Enter the interrupt service routine to clear the interrupt and return. 4. Continue executing subsequent instructions.

5 EFC

5.1 Main Features

- Supporting EFLASH operations including 8-bit read/write and sector erase
- Configurable read wait time
- Main memory consists of 128 sectors, each with 512 bytes
- Erase/write protection
- Automatic bus locking
- Maximum operation time: sector erase (19 ms), chip erase (70 ms), word write (70 μs), read (25 ns)

5.2 EFLASH Read Efficiency

When the RD_WAIT value is set to 0, there is no efficiency loss during CPU instruction fetching, and the timing of reading EFLASH is the same as that of reading ROM at the controller side. When the RD_WAIT value is set to 1, the EFC bus will be pulled low for one cycle during each read operation.

5.3 Parameter Address

SN number acquisition address: 0x9248, size: 16 bytes

VCAP acquisition address: 0x919C; size: 4 bytes

5.4 Register Description

Table 5-1: List of Registers

Address	Name	Description
A7H	EFC_OPSET	Setting register
A3H	OINTUS	Interrupt status register
D1H~D2H	EFC_OADRL/H	EFLASH programming address register
D3H	EFC_ODATA	EFLASH programming data register
D4H	EFC_OCTRL	Voltage output register
A2H	OINTEN	Interrupt enable register

5.4.1 EFC_OPSET Setting Register

A7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EFC_OPSET	EEPROM_SET	NVR_SET	RDWAIT			CHIPSERSET	PAGESERSET	PAGEWRSET
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	1

Bit No.	Bit Designator	Description
7	EEPROM_SET	Enable bit for erasing and writing the last 4KB memory of Flash main area in Boot mode
6	NVR_SET	Enable bit for erasing and writing the EEPROM area
5:3	RDWAIT	Setting bit for read wait time
2	CHIPSERSET	1: Enable CHIP erase mode 0: Disable CHIP erase mode
1	PAGESERSET	1: Enable PAGE erase mode 0: Disable PAGE erase mode
0	PAGEWRSET	1: Enable PAGE write mode 0: Disable PAGE write mode

5.4.2 OINTUS Interrupt Status Register

A3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OINTUS	-	NVRCERR	VDD_LOW	WPOGERR	BOOTERR	NVR1ERR	NVR0ERR	PRODONE

R/W	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	-	-
6	NVRCERR	1: NVRC error interrupt status bit 0: NVRC error interrupt status bit Write 1 to clear this bit.
5	VDD_LOW	1: LVD interrupt status bit 0: LVD interrupt status bit Write 1 to clear this bit.
4	WPOGERR	1: Operation error interrupt status bit 0: Operation error interrupt status bit Write 1 to clear this bit.
3	BOOTERR	1: BOOT error interrupt status bit 0: BOOT error interrupt status bit Write 1 to clear this bit.
2	NVR1ERR	1: NVR1 error interrupt status bit 0: NVR1 error interrupt status bit Write 1 to clear this bit.
1	NVR0ERR	1: NVR0 error interrupt status bit 0: NVR0 error interrupt status bit Write 1 to clear this bit.
0	PRODONE	1: Erase/write complete interrupt status bit 0: Erase/write complete interrupt status bit Write 1 to clear this bit.

5.4.3 EFC_OADRL/H EFLASH Programming Address Register

D1H-D2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EFC_OADRL	Lower 8 bits [7:0] of EFLASH programming address							
EFC_OADRH	Upper 8 bits [15:8] of EFLASH programming address							
R/W	R/W							
Reset Value	1	1	1	1	1	1	1	1

5.4.4 EFC_ODATA EFLASH Programming Data Register

D3H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EFC_ODATA	EFLASH programming data [7:0]							
R/W	R/W							
Reset Value	1	1	1	1	1	1	1	1

5.4.5 EFC_OCTRL Voltage Output Register

D4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
EFC_OCTRL	VPPO_EN	PUMP_EN	PUMP_SEL<2:0>			-	PUMP_OK	PUMP_6O5V
R/W	R/W	R/W	R/W			-	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	VPPO_EN	EFLASH IAP startup control signal: 0: Disabled (automatically cleared to 0 by hardware) 1: Start EFLASH programming (software writes 1 to start EFLASH IAP and hardware clears this bit to 0 upon completion of IAP.) After this bit is set, CPU will enter the Idle state and resume normal operation upon completion of IAP.
6	PUMP_EN	PUMP module enable bit: 0: Disable the internal PUMP function. 1: Enable the internal PUMP function.
5:3	PUMP_SEL<2:0>	Pump output voltage selection control bit: PUMP_SEL / VPP (V) / PUMP_SEL / VPP (V) 000 / 6.5 / 100 / 7.5 001 / 6.75 / 101 / 7.75 010 / 7.0 / 110 / 8 011 / 7.25 / 111 / 8.25 It is recommended to set PUMP_SEL<2:0> = 001 (corresponding to 6.75 V) for actual IAP programming.
2	-	-

1	PUMP_OK	VPP output voltage flag 1: 0: VPP OUT voltage is lower than the voltage set by PUMP_SEL. 1: VPP OUT voltage is higher than the voltage set by PUMP_SEL.
0	PUMP_6O5V	VPP output voltage flag 2: 1: VPP OUT voltage is higher than 6.5 V. 0: VPP OUT voltage is lower than 6.5 V.

5.4.6 OINTEN Interrupt Enable Register

A2H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OINTEN	-	NVRCERREN	VDDLOWEN	WPOGERREN	BOOTERREN	NVR1ERREN	NVR0ERREN	PRODONEEN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	-	-
6	NVRCERREN	1: NVRC error interrupt enabled 0: NVRC error interrupt disabled
5	VDDLOWEN	1: LVD interrupt enabled 0: LVD interrupt disabled
4	WPOGERREN	1: Operation error interrupt enabled 0: Operation error interrupt disabled
3	BOOTERREN	1: BOOT error interrupt enabled 0: BOOT error interrupt disabled
2	NVR1ERREN	1: NVR1 error interrupt enabled 0: NVR1 error interrupt disabled
1	NVR0ERREN	1: NVR0 error interrupt enabled 0: NVR0 error interrupt disabled
0	PRODONEEN	1: Write/erase done interrupt enabled 0: Write/erase done interrupt disabled

5.5 Software Process

5.5.1 Read Operation

EFLASH can perform read operation as it is stabilized after power-on. Pay attention to configure the read wait time RD_WAIT for the read operation.

5.5.2 Write Operation

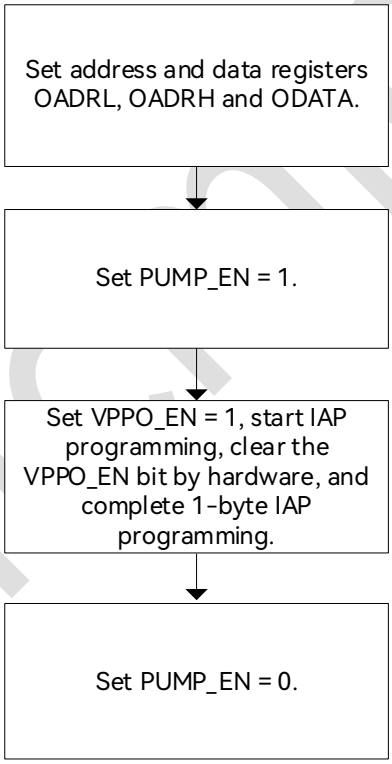


Figure 5-1: Write Operation Process

5.5.3 Erase Operation

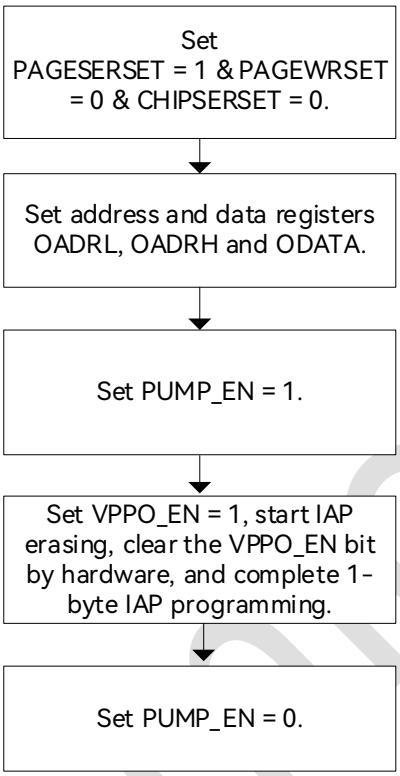


Figure 5-2: Erase Operation Process

5.5.4 Chip Erase Operation

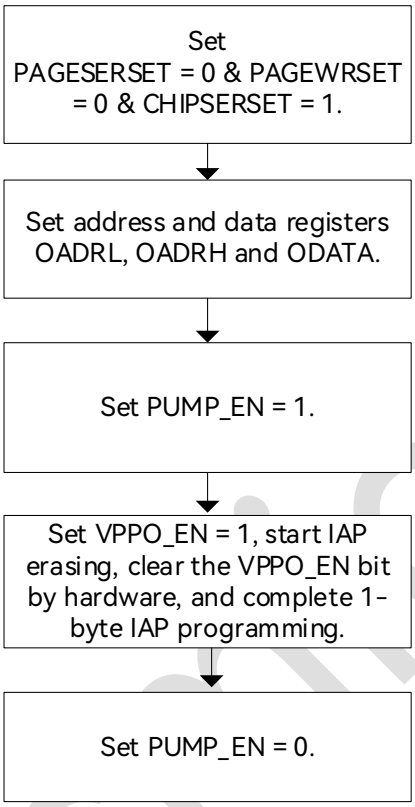


Figure 5-3: Chip Erase Operation Process

6 Pulse Width Modulation (PWM) Module

6.1 Main Features

- 11-channel 16-bit PWM module
- Providing overflow interrupt for each PWM cycle
- Output polarity selection

6.2 Functional Description

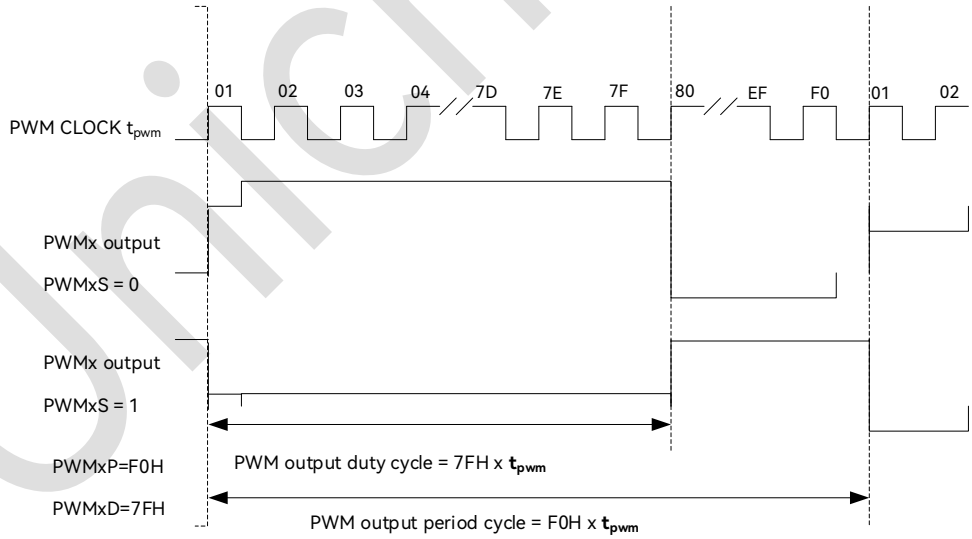


Figure 6-1: PWM Output Example

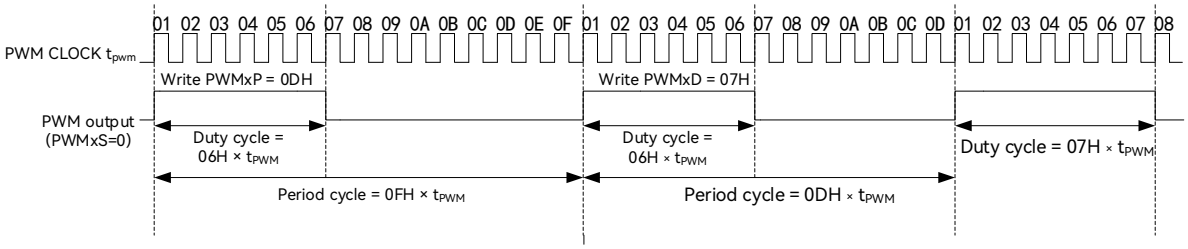


Figure 6-2: Example of PWM Output Cycle or Duty Cycle Change

6.3 PWM Output Timing

Table 6-1: Output Timing (PWMxSS = 1)

PWMxS	Condition	PWMx Port Output Status
0	PWMxP > PWMxD	Output a square wave: first output a high level for PWMxD clock cycles, then output a low level for (PWMxP - PWMxD) clock cycles.
	PWMxP ≤ PWMxD	High level
	PWMxD = 0, PWMxP = 0	High level
	PWMxD = 0, PWMxP ≠ 0	Low level
1	PWMxP > PWMxD	Output a square wave: first output a low level for PWMxD clock cycles, then output a high level for (PWMxP - PWMxD) clock cycles.
	PWMxP ≤ PWMxD	Low level
	PWMxD = 0, PWMxP = 0	Low level
	PWMxD = 0, PWMxP ≠ 0	High level

Notes:

- The PWMxEN bit controls the on/off of the PWMx module.
- The PWMxSS (x = 0–2) bit can select whether the port functions as an I/O port or a PWM output port. If PWMxSS = 1 but PWMxEN = 0, the corresponding port is in the input state.
- The EPWM bit in the IENO register and the PWMxIE bit in the PWMxCON register jointly control the PWMx interrupt.
- The three PWM modules share a common interrupt vector.
- When PWMENx = 1 and PWMxSS = 0, the PWMx module output is disabled, and the PWM

module can be used as a 16-bit timer. If the PWM interrupt is enabled and PWMxIE = 1, an interrupt will also be triggered for each PWM cycle.

6.4 Register Description

Table 6-2: List of Registers

Address	Name	Description
CBH	PWM0_PL	PWM0 data register
CCH	PWM0_PH	PWM0 data register
CDH	PWM1_PL	PWM1 data register
CEH	PWM1_PH	PWM1 data register
C1H	PWM2_PL	PWM2 data register
C2H	PWM2_PH	PWM2 data register
C3H	PWM0_DL	PWM0 duty cycle control register
C4H	PWM0_DH	PWM0 duty cycle control register
C5H	PWM1_DL	PWM1 duty cycle control register
C6H	PWM1_DH	PWM1 duty cycle control register
CFH	PWM2_DL	PWM2 duty cycle control register
C7H	PWM2_DH	PWM2 duty cycle control register
C8H	PWM0_CON	PWM0 setting register
C9H	PWM1_CON	PWM1 setting register
CAH	PWM2_CON	PWM2 setting register

6.4.1 PWMx_PL/H PWMx Data Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0_PL (CBH)	PWM0P[7:0]							
PWM0_PH (CCH)	PWM0P[15:8]							
PWM1_PL (CDH)	PWM1P[7:0]							
PWM1_PH (CEH)	PWM1P[15:8]							
PWM2_PL (C1H)	PWM2P[7:0]							
PWM2_PH (C2H)	PWM2P[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
15:0	PWMxP[15:0] (x = 0, 1, 2)	PWMx data register

Note:

- Modifying the register PWMxPH will make the output of PWMx take effect in the next cycle.
- If the PWM period is required to be modified, first modify PWMxPL and then PWMxPH.

6.4.2 PWMx_DL/H PWMx Duty Cycle Control Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0_DL (C3H)	PWM0D[7:0]							
PWM0_DH (C4H)	PWM0D[15:8]							
PWM1_DL (C5H)	PWM1D[7:0]							
PWM1_DH (C6H)	PWM1D[15:8]							
PWM2_DL (CFH)	PWM2D[7:0]							
PWM2_DH (C7H)	PWM2D[15:8]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
15:0	PWMxD[15:0] (x = 0, 1, 2)	PWMx duty cycle control, controlling the output time of PWM0 waveform duty cycle. For detailed PWM output timing, please refer to the Chapter PWM Output Timing.

Note:

- Modifying the register PWMxDH will make the output of PWMx take effect in the next cycle.
- If the PWM period is required to be modified, first modify PWMxDL and then PWMxDH.

6.4.3 PWMx_CON PWMx Setting Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PWM0_CON (C8H)	PWM0EN	PWM0S	-	-	-	PWM0IE	PWM0IF	PWM0SS
PWM1_CON (C9H)	PWM1EN	PWM1S	-	-	-	PWM1IE	PWM1IF	PWM1SS

PWM2_CON (CAH)	PWM2EN	PWM2S	-	-	-	PWM2IE	PWM2IF	PWM2SS
R/W	R/W	R/W	-	-	-	R/W	R/W	R/W
Reset Value	0	0	-	-	-	0	0	0

Bit No.	Bit Designator	Description
7	PWMxEN	PWMx enable: 0: Disable the PWMx module 1: Enable the PWMx module
6	PWMxS	PWMx output mode: 0: Output high level during PWMx duty cycle, and output low level after duty cycle overflow 1: Output low level during PWMx duty cycle, and output high level after duty cycle overflow
5:3	-	-
2	PWMxIE	PWMx interrupt enable bit: 0: Disable PWMx interrupt 1: Enable PWMx interrupt The three PWM modules share a common interrupt vector address.
1	PWMxIF	PWMx interrupt flag bit: 0: The PWM period counter has not overflowed. 1: The PWMx period counter has overflowed. This bit is set by hardware. Writing 1 by software is invalid, while writing 0 clears the bit.
0	PWMxSS	PWMx pin output control bit: 0: Disable P1_0 as PWM0 output, P1_1 as PWM1 output, and P1_2 as PWM2 output. These pins will function as I/O. 1: Enable P1_0 as PWM0 output, P1_1 as PWM1 output, and P1_2 as PWM2 output. **Note:** ● Set this bit when PWM0_OUT is assigned to P1_0, PWM1_OUT to P1_1, and PWM2_OUT to P1_2. ● This bit is not required to be set when PWM0_OUT is assigned to P1_1/P2_0, PWM1_OUT to P1_2/P1_5, and PWM2_OUT to P1_3.

6.5 Software Operation Process

1. Configure the PWM output pin by setting the PWMxSS bit or enabling the corresponding pin alternate function.
2. Write the PWMx_PL/PH bit to set the PWM period.
3. Write the PWMx_DL/DH bit to set the PWM duty cycle.
4. Write the PWMxS bit to configure the PWM output polarity.
5. If interrupt is to be used, first write the EAL and EPWM bits, then write the PWMxIE register to enable PWM interrupt.
6. Finally, write the PWMxEN bit to enable the PWM module.

7 GPIO (I/O Port)

7.1 Main Features

- Up to 17 programmable bidirectional I/O ports
- All I/O ports support interrupt triggered by either edge
- Built-in pull-up resistor
- I/O port with alternate functions

7.2 Port Module Diagram

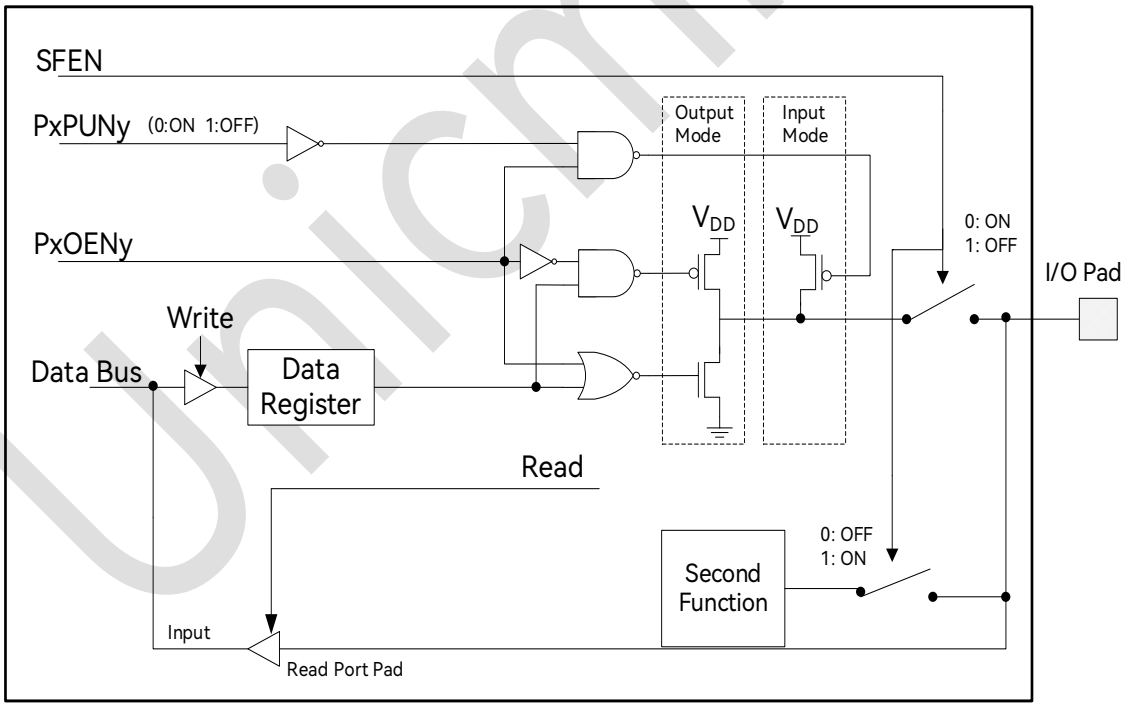


Figure 7-1: Port Module Diagram

Note:

- Reading an I/O port configured as an input directly reads the pin level.
- Reading an I/O port configured as an output also reads the pin level.

- Even if the I/O port is configured for other alternate functions, writing to the port is always directed to the port data register.

7.3 Port Interrupt

All ports support interrupt functions. If the interrupt is enabled, either rising or falling edge will trigger the interrupt, and all port interrupts share the INT0 interrupt entry. The edge triggering the interrupt for I/O ports is configured by writing to the P0AL/P0AH/P1AL/P1AH/P2AL/P2AH registers.

The PxIEN register controls the enabling and disabling of interrupts for all I/O ports. If the interrupt of a certain port is enabled, the MCU will generate an external interrupt and set the corresponding PxIRQ flag to 1 when it detects a rising or falling edge on the pin. The user program can query which pin has generated the interrupt flag within the service routine of external interrupt 0.

If the port interrupt is enabled, the change in port level can generate interrupt to wake up the MCU from power-down mode.

7.4 Register Description

Table 7-1: Register Configuration

Address	Name	Description
C010H	P00_CFG	Port P0_0 function configuration register
C011H	P01_CFG	Port P0_1 function configuration register
C013H	P03_CFG	Port P0_3 function configuration register
C014H	P04_CFG	Port P0_4 function configuration register
C018H	P10_CFG	Port P1_0 function configuration register
C019H	P11_CFG	Port P1_1 function configuration register
C01AH	P12_CFG	Port P1_2 function configuration register
C01BH	P13_CFG	Port P1_3 function configuration register

Address	Name	Description
C01CH	P14_CFG	Port P1_4 function configuration register
C01DH	P15_CFG	Port P1_5 function configuration register
C020H	P20_CFG	Port P2_0 function configuration register
C022H	P22_CFG	Port P2_2 function configuration register
C023H	P23_CFG	Port P2_3 function configuration register
C025H	P25_CFG	Port P2_5 function configuration register
C026H	P26_CFG	Port P2_6 function configuration register
C027H	P27_CFG	Port P2_7 function configuration register
C000H	P0_IE	P0 IO input control register
C001H	P1_IE	P1 IO input control register
C002H	P2_IE	P2 IO input control register
C005H	P0_SR	P0 IO speed control register
C006H	P1_SR	P1 IO speed control register
C007H	P2_SR	P2 IO speed control register

7.4.1 P00_CFG

C010H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P00_CFG	-	-	-	-	-	P00_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P00_SEL	000: P0_0 001: UART2_RX 010: SPI_CSN 011: LPOUT0 100: GTIMER1_CHN 101: GTIMER2_BKE 110: -

7.4.2 P01_CFG

C011H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P01_CFG	-	-	-	-	-	P01_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P01_SEL	000: P0_1 001: UART2_TX 010: SPI_SCK 011: I2C_SDA 100: LPOUT1 101: GTIMER0_BKE 110: GTIMER2_CHN 111: -

7.4.3 P03_CFG

C013H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P03_CFG	-	-	-	-	-	P03_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x01		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P03_SEL	000: P0_3 001: CLKOUT 010: UART2_TX 011: UART3_RX 100: SPI_CSN 101: LPOUT0 110: GTIMER1_CH 111: -

7.4.4 P04_CFG

C014H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P04_CFG	-	-	-	-	-	P04_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x03		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P04_SEL	000: P0_4 001: UART2_RX 010: SPI_SCK 011: I2C_SDA 100: LPOUT1 101: GTIMER1_BKE 110: GTIMER2_CHN 111: -

7.4.5 P10_CFG

C018H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P10_CFG	-	-	-	-	-	P10_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x04		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P10_SEL	000: P1_0 001: UART1_RX 010: UART2_TX 011: PWM0 100: I2C_SCL 101: LP0_IN 110: GTIMER2_CH 111: UART2_RX

7.4.6 P11_CFG

C019H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P11_CFG	-	-	-	-	P11_SEL			
R/W	R	R	R	R	R/W			
Reset Value	0	0	0	0	0			

Bit No.	Bit Designator	Description
7:3	-	-
3:0	P11_SEL	0000: P1_1 0001: UART1_TX 0010: UART3_RX 0011: PWM1 0100: SPI_MISO 0101: LP0_TRG 0110: GTIMER1_CHN 0111: PWM0 1000–1110: Reserved 1111: UART2_TX

7.4.7 P12_CFG

C01AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P12_CFG	-	-	-	-	-	P12_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P12_SEL	000: P1_2 001: UART0_RX 010: UART3_TX 011: PWM2 100: LP0_CAP 101: GTIMER1_CH 110: PWM1 111: -

7.4.8 P13_CFG

C01BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P13_CFG	-	-	-	-	-	P13_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P13_SEL	000: P1_3 001: UART0_TX 010: UART2_RX 011: SPI_SCK 100: I2C_SDA 101: LP0_IN 110: GTIMER0_CH 111: PWM2

7.4.9 P14_CFG

C01CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P14_CFG	-	-	-	-	-	P14_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x01		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P14_SEL	000: P1_4 001: UART1_RX 010: PWM2 011: SPI_MOSI 100: LP0_TRG 101: GTIMER0_CHN 110: GTIMER1_BKE 111: -

7.4.10 P15_CFG

C01DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P15_CFG	-	-	-	-	-	P15_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x01		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P15_SEL	000: P1_5 001: UART1_TX 010: PWM1 011: SPI_MISO 100: GTIMER0_CH 101: GTIMER1_BKE 110: GTIMER2_CH 111: LP0_CAP1

7.4.11 P20_CFG

C020H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P20_CFG	-	-	-	-	-	P20_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P20_SEL	000: P2_0 001: UART3_RX 010: PWM0 011: SPI_MOSI 100: I2C_SCL 101: LPOUT0 110: GTIMER0_CHN

7.4.12 P22_CFG

C022H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P22_CFG	-	-	-	-	-	P22_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P22_SEL	000: P2_2 001: UART3_TX 010: SPI_CSN 011: SPI_MISO 100: I2C_SDA 101: GTIMER0_BKE 110: GTIMER2_CHN 111: LP0_CAP1

7.4.13 P23_CFG

C023H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P23_CFG	-	-	-	-	-	P23_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P23_SEL	000: P2_3 001: UART3_RX 010: SPI_SCK 011: SPI_MOSI 100: LP0_CAP 101: GTIMER0_CHN 110: GTIMER2_BKE 111: -

7.4.14 P25_CFG

C025H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P25_CFG	-	-	-	-	-	P25_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x06		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P25_SEL	000: P2_5 001: UART3_TX 010: SPI_CSN 011: I2C_SCL 100: GTIMER0_CH 101: GTIMER0_BKE 110: BUZZER_OUT 111: UART0_RX

7.4.15 P26_CFG

C026H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P26_CFG	-	-	-	-	-	P26_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x01		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P26_SEL	000: P2_6 001: UART0_TX 010: UART2_TX 011: SPI_MISO 100: LPOUT1 101: GTIMER1_CH 110: GTIMER2_CH

7.4.16 P27_CFG

C027H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P27_CFG	-	-	-	-	-	P27_SEL		
R/W	R	R	R	R	R	R/W		
Reset Value	0	0	0	0	0	0x01		

Bit No.	Bit Designator	Description
7:3	-	-
2:0	P27_SEL	000: P2_7 001: UART0_RX 010: UART2_RX 011: SPI_MOSI 100: I2C_SCL 101: GTIMER1_CHN 110: GTIMER2_BKE 111: BUZZER_OUT

7.4.17 P0_IE

C000H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0_IE	-	-	-	P0_4_IE	P0_3_IE	P0_2_IE	P0_1_IE	P0_0_IE
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:5	-	-
4	P0_4_IE	P0_4 IO input control bit: 0: P0_4 input disabled 1: P0_4 input enabled
3	P0_3_IE	P0_3 IO input control bit: 0: P0_3 input disabled 1: P0_3 input enabled
2	P0_2_IE	P0_2 IO input control bit: 0: P0_2 input disabled 1: P0_2 input enabled

1	P0_1_IE	P0_1 IO input control bit: 0: P0_1 input disabled 1: P0_1 input enabled
0	P0_0_IE	P0_0 IO input control bit: 0: P0_0 input disabled 1: P0_0 input enabled

7.4.18 P1_IE

C001H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1_IE	-	-	P1_5_IE	P1_4_IE	P1_3_IE	P1_2_IE	P1_1_IE	P1_0_IE
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	0	1

Bit No.	Bit Designator	Description
7:6	-	-
5	P1_5_IE	P1_5 IO input control bit: 0: P1_5 input disabled 1: P1_5 input enabled
4	P1_4_IE	P1_4 IO input control bit: 0: P1_4 input disabled 1: P1_4 input enabled
3	P1_3_IE	P1_3 IO input control bit: 0: P1_3 input disabled 1: P1_3 input enabled
2	P1_2_IE	P1_2 IO input control bit: 0: P1_2 input disabled 1: P1_2 input enabled
1	P1_1_IE	P1_1 IO input control bit: 0: P1_1 input disabled 1: P1_1 input enabled
0	P1_0_IE	P1_0 IO input control bit: 0: P1_0 input disabled 1: P1_0 input enabled

7.4.19 P2_IE

C002H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2_IE	P2_7_IE	P2_6_IE	P2_5_IE	-	P2_3_IE	P2_2_IE	-	P2_0_IE
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	1	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	P2_7_IE	P2_7 IO input control bit: 0: P2_7 input disabled 1: P2_7 input enabled
6	P2_6_IE	P2_6 IO input control bit: 0: P2_6 input disabled 1: P2_6 input enabled
5	P2_5_IE	P2_5 IO input control bit: 0: P2_5 input disabled 1: P2_5 input enabled
4	-	-
3	P2_3_IE	P2_3 IO input control bit: 0: P2_3 input disabled 1: P2_3 input enabled
2	P2_2_IE	P2_2 IO input control bit: 0: P2_2 input disabled 1: P2_2 input enabled
1	-	-
0	P2_0_IE	P2_0 IO input control bit: 0: P2_0 input disabled 1: P2_0 input enabled

7.4.20 P0_SR

C005H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P0_SR	-	-	-	P0_4_SR	P0_3_SR	P0_2_SR	P0_1_SR	P0_0_SR
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	1	1	1	1	1

Bit No.	Bit Designator	Description
7:5	-	-
4	P0_4_SR	P0_4 IO speed control bit: 0: P0_4 fast 1: P0_4 slow
3	P0_3_SR	P0_3 IO speed control bit: 0: P0_3 fast 1: P0_3 slow
2	P0_2_SR	P0_2 IO speed control bit: 0: P0_2 fast 1: P0_2 slow
1	P0_1_SR	P0_1 IO speed control bit: 0: P0_1 fast 1: P0_1 slow
0	P0_0_SR	P0_0 IO speed control bit: 0: P0_0 fast 1: P0_0 slow

7.4.21 P1_SR

C006H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P1_SR	-	-	P1_5_SR	P1_4_SR	P1_3_SR	P1_2_SR	P1_1_SR	P1_0_SR
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7:6	-	-
5	P1_5_SR	P1_5 IO speed control bit: 0: P1_5 fast 1: P1_5 slow
4	P1_4_SR	P1_4 IO speed control bit: 0: P1_4 fast 1: P1_4 slow
3	P1_3_SR	P1_3 IO speed control bit: 0: P1_3 fast 1: P1_3 slow
2	P1_2_SR	P1_2 IO speed control bit:

		0: P1_2 fast 1: P1_2 slow
1	P1_1_SR	P1_1 IO speed control bit: 0: P1_1 fast 1: P1_1 slow
0	P1_0_SR	P1_0 IO speed control bit: 0: P1_0 fast 1: P1_0 slow

7.4.22 P2_SR

C007H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
P2_SR	P2_7_SR	P2_6_SR	P2_5_SR	-	P2_3_SR	P2_2_SR	-	P2_0_SR
R/W	R/W	R/W	R/W	R	R/W	R/W	R	R/W
Reset Value	1	1	1	0	1	1	0	1

Bit No.	Bit Designator	Description
7	P2_7_SR	P2_7 IO speed control bit: 0: P2_7 fast 1: P2_7 slow
6	P2_6_SR	P2_6 IO speed control bit: 0: P2_6 fast 1: P2_6 slow
5	P2_5_SR	P2_5 IO speed control bit: 0: P2_5 fast 1: P2_5 slow
4	-	-
3	P2_3_SR	P2_3 IO speed control bit: 0: P2_3 fast 1: P2_3 slow
2	P2_2_SR	P2_2 IO speed control bit: 0: P2_2 fast 1: P2_2 slow
1	-	-
0	P2_0_SR	P2_0 IO speed control bit: 0: P2_0 fast 1: P2_0 slow

8 Beeper

The chip integrates a beeper signal generator that can automatically output square waves of 1 kHz, 2 kHz and 4 kHz via hardware.

8.1 Register Description

8.1.1 BEEPCTR

86H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
BEEPCTR	UART3CEN	UART3RSTEN	-	BEEPEN	-	BEEPCOLSET	BEEPSEL[1:0]	
R/W	R/W	R/W	R	R/W	R	R/W	R/W	
Reset Value	1	1	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	UART3CEN	1: UART3 clock enabled 0: UART3 clock disabled
6	UART3RSTEN	1: UART3 reset released 0: UART3 reset
5	-	-
4	BEEPEN	BEEP module enable bit: 0: BEEP module disabled 1: BEEP module enabled Note: BEEP defaults to P2.5 output.
3	-	-
2	BEEPCOLSET	BEEP polarity control: 0: BEEP outputs low level by default 1: BEEP outputs high level by default
1:0	BEEPSEL	BEEP output frequency control: 00/11: 1 kHz 01: 2 kHz 10: 4 kHz

9 UART0/1 (Enhanced Serial Port)

9.1 Main Features

- Both UART0 and UART1 come with baud rate generators.
- UART0 supports four operating modes.
- UART1 supports two operating modes.

Both serial ports consists of a shift register, a serial control register, a baud rate generator, and two independent data buffers (for transmitting and receiving data respectively). The two data buffers are collectively referred to as S0BUF (S1BUF), sharing the address 99H (9CH). Writing data to S0BUF or S1BUF initiates the serial data transmission, while reading S0BUF or S1BUF returns the data that has been received by the buffer.

When the serial port is receiving data, the data first enters the shift register. After a complete frame of data is received, the data is shifted into S0BUF (or S1BUF), and the serial port immediately starts receiving the next frame of data. The master must ensure that the data in the S0BUF (or S1BUF) buffer is read out before the reception of the current frame is completed; otherwise, the previous frame of data will be overwritten by current frame, resulting in data loss.

9.2 UART0 Operating Mode

UART0 supports four operating modes. Before communication, the user must initialize the relevant registers and select the appropriate operating mode and baud rate. Different operating modes can be selected by setting SM0/SM1.

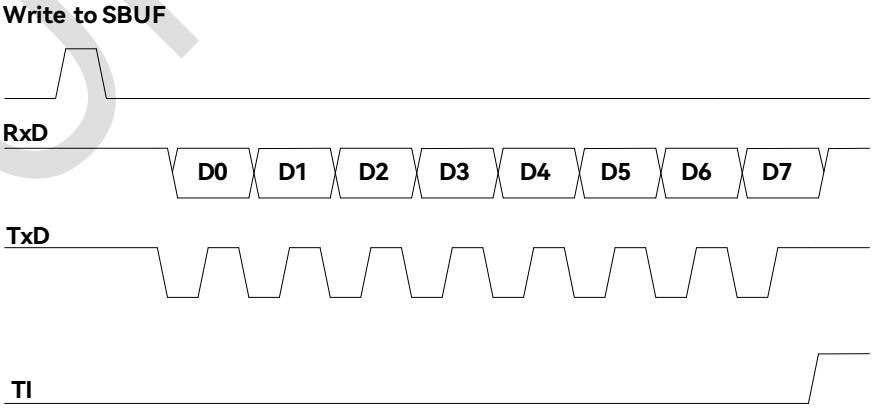
Table 9-1: List of UART0 Operating Mode

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	SYSCLK / 12
0	1	1	8-bit UART	Configurable
1	0	2	9-bit UART	SYSCLK / 16
1	1	3	9-bit UART	Configurable

- Mode 0: synchronous, half-duplex communication

  Mode 0 supports synchronous communication with external devices. Serial data is received and transmitted via the RX pin, while the TX pin sends the shift clock. In this mode, 8 bits are transmitted and received per frame, with the least significant bit (LSB) being received or transmitted first.

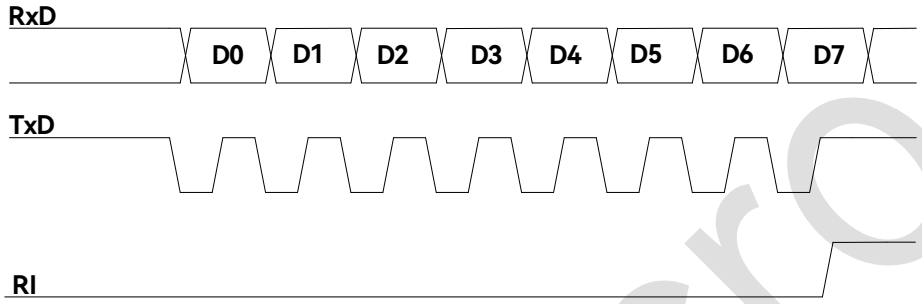
  Any write operation targeting the SBUF register initiates transmission. The TX control module starts transmitting data on the next system clock cycle. Data conversion occurs on the falling edge of the shift clock, shifting the contents of the shift register sequentially from left to right, with the null bits set to 0. Upon completion of transmission, the TX control module stops transmitting and then sets the TI flag bit on the rising edge of the next system clock.



Transmit Timing of Mode 0

Initialize reception by setting REN to 1 and clearing RI to 0. Data is latched on the rising

edge of the shift clock, and the contents of the receive shift register are shifted to the left sequentially. After all 8 bits of data have been shifted into the shift register, the RX control module stops receiving. RI is set on the rising edge of the next system clock, and subsequent reception is allowed only after software clears it.

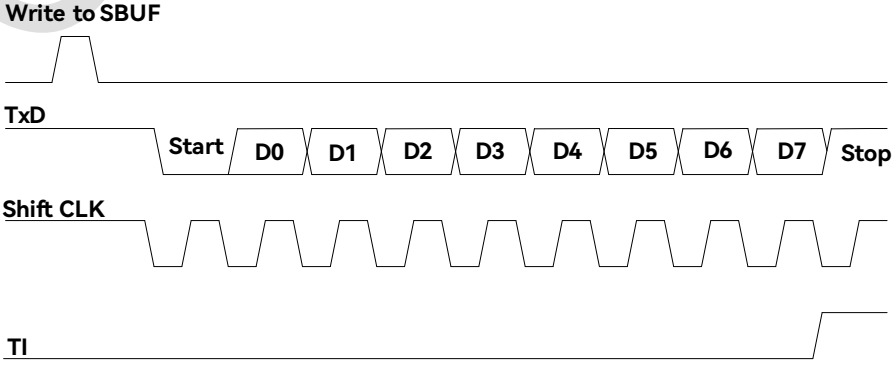


Receive Timing of Mode 0

- Mode 1: 8-bit UART, variable baud rate, asynchronous full-duplex

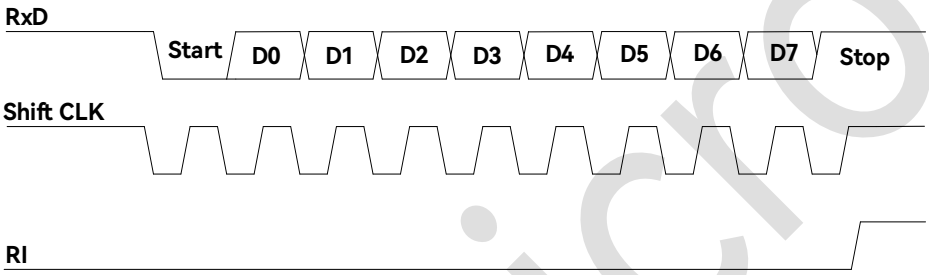
Mode 1 supports 10-bit full-duplex asynchronous communication. The 10 bits consists of one start bit (logic 0), eight data bits (LSB bit), and one stop bit (logic 1). During reception, the 8 data bits are stored in SBUF, and the stop bit is stored in RB8.

Any write operation targeting the SBUF register initiates transmission, with the start bit first shifted out on the TX pin, followed by the 8 data bits. After all 8 data bits in the transmit shift register are transmitted, the stop bit is shifted out on the TX pin, and the TI flag is set to issue an interrupt request at the same time as the stop bit is transmitted.



Transmit Timing of Mode 1

Reception is allowed only when REN is set. The serial port starts receiving serial data when the RX pin detects a falling edge. If the start bit is valid, it is shifted into the shift register, followed by the subsequent bits. After the 8 data bits and 1 stop bit are shifted in, the contents of the shift register are loaded into SBUF and RB8 respectively, and then RI is set. At this point, the receiver continues to detect the next falling edge on RX pin. The user shall clear RI by software before resuming reception.

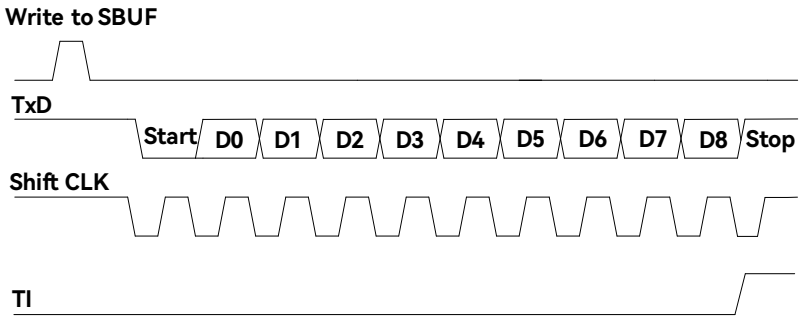


Receive Timing of Mode 1

- Mode 2: 9-bit UART, fixed baud rate, asynchronous full-duplex

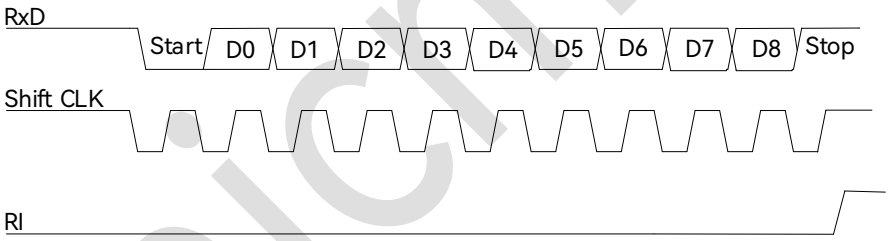
Mode 2 supports 11-bit full-duplex asynchronous communication with a fixed baud rate of 1/16 of the system clock. A frame consists of one start bit (logic 0), eight data bits (LSB first), one programmable 9th bit, and one stop bit (logic 1). Mode 2 and Mode 3 support multi-machine communication.

Any write operation targeting the SBUF register initiates transmission, and TB8 is loaded into bit 9 of the transmit shift register simultaneously. The start bit is first shifted out on the TX pin, followed by the 9 data bits. After all the data are transmitted, the stop bit is shifted out on the TX pin, and the TI flag is set to issue an interrupt request as the stop bit starts to be transmitted.



Transmit Timing of Mode 2

Reception is allowed only when REN is set. The serial port starts receiving serial data when a falling edge is detected on the RX pin. If the start bit is valid, it is shifted into the shift register, followed by the subsequent bits. After the 9 data bits and 1 stop bit are shifted in, the contents of the shift register are loaded into SBUF and RB8 respectively, and then RI is set. At this point, the receiver continues to detect the next falling edge on RX pin. The user shall clear RI by software before resuming reception.



Receive Timing of Mode 2

- Mode 3: 9-bit UART, variable baud rate, asynchronous full-duplex

  Mode 3 adopts the transmission protocol of Mode 2 and the baud rate generation method of Mode 1.

Note: For serial port I/O, the internal pull-up of the corresponding IO must be enabled in the PxPUN register; otherwise, the RX pin will be in a floating state and susceptible to interference.

9.3 UART1 Operating Mode

Table 9-2: List of UART1 Operating Mode

SM	Mode	Description	Baud Rate
0	A	9-bit UART	Configurable
1	B	8-bit UART	Configurable

Mode A and Mode B of UART1 refer to Mode 3 and Mode 1 of UART0 respectively.

9.4 Multi-machine Communication

Mode 2 and Mode 3 of UART0, as well as Mode A of UART1, support multi-machine communication. In a multi-machine communication system, when the master intends to send a data block to one of multiple slaves, it first transmits an address byte to address the target slave. The address byte and the data byte can be distinguished by the 9th data bit, which is 1 for the address byte and 0 for the data byte. The receiver determines whether to receive data based on the information of the 9th bit. The multi-machine communication process is as follows:

- Master transmitting process:
  1. Set to the 9-bit mode, send the receiver address, and set TB8 = 1.
  2. Transmit the data according to the custom protocol, and set TB8 = 0.
- Master receiving process:
  1. Set SM2 = 0 (unconditionally receive all data).
  2. The master parses the data according to the custom protocol.
- Slave receiving process:
  1. Set SM2 = 1 for the slave to be in the state of only receiving address frames, at this time only the address data with the 9th bit being 1 will be received.

2. When the data is received, the software determines whether it matches the serial port address configured for the local machine.

3. After all slaves receive the address frame, each compares the received address with its own address.

   - If there is a match (indicating it is the target slave), set SM2 = 0, prepare to receive the data frame that the master is about to send, and set SM2 = 1 again after receiving.
   - If there is no match, keep SM2 = 1, and ignore all subsequent data frames without generating interrupt requests until an address frame is received again for comparison and confirmation.

9.5 UART0 Register Description

Table 9-3: List of Registers

Address	Name	Description
98H	UART0_S0CON	Interrupt register
AAH	UART0_S0RELL	Baud rate configuration register
BAH	UART0_S0RELH (BAH)	Baud rate configuration register
99H	UART0_S0BUF	Data register
9EH	UARTEN	Enable register

9.5.1 UART0_S0CON Interrupt Register

98H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART0_S0CON	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	SM0	UART0 mode selection bit:

6	SM1	<table><tr><th>SM0</th><th>SM1</th><th>T0MODE</th><th>Description</th><th>Baud Rate</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Shift register</td><td>SYSCLK / 12</td></tr><tr><td>0</td><td>1</td><td>1</td><td>8-bit UART</td><td>Configurable</td></tr><tr><td>1</td><td>0</td><td>2</td><td>9-bit UART</td><td>SYSCLK / 16</td></tr><tr><td>1</td><td>1</td><td>3</td><td>9-bit UART</td><td>Configurable</td></tr></table>
5	SM20	UART0 multi-machine communication enable bit: 0: Disable the multi-machine communication function. 1: Enable the multi-machine communication to receive only 9-bit data with RB80 = 1.
4	REN0	UART0 receive enable bit: 0: Disable data reception on UART0. 1: Enable data reception on UART0.
3	TB80	The 9th transmit data bit in Mode 2 and Mode 3 of UART0
2	RB80	The 9th receive data bit in Mode 2 and Mode 3 of UART0
1	TI0	UART0 transmit interrupt flag bit: Upon completion of data transmission, this bit shall be set by hardware and must be cleared by software.
0	RI0	UART0 receive interrupt flag bit: Upon completion of data reception, this bit shall be set by hardware and must be cleared by software.

9.5.2 UART0_S0REL Baud Rate Configuration Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART0_S0RELL (AAH)	S0RELL.7	S0RELL.6	S0RELL.5	S0RELL.4	S0RELL.3	S0RELL.2	S0RELL.1	S0RELL.0
Reset Value	1	1	1	0	0	1	1	0
UART0_S0RELH (BAH)	-	-	-	-	-	-	S0RELH.1	S0RELH.0
Reset Value	-	-	-	-	-	-	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit No.	Bit Designator	Description
7:0 1:0	S0RELL[7:0] S0REH[1:0]	Baud rate configuration register for Mode 1 and Mode 3 of UART0: S0RELH + S0RELL constitute the baud rate setting S0REL[9:0] Baud rate = $\frac{\text{SYSCK}}{16\times(1024-\text{S0REL})}$

9.5.3 UART0_S0BUF Data Register

99H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART0_S0BUF	S0BUF.7	S0BUF.6	S0BUF.5	S0BUF.4	S0BUF.3	S0BUF.2	S0BUF.1	S0BUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	S0BUF[7:0]	UART0 data register: Reading S0BUF returns the data received by UART0. Writing to S0BUF initiates data transmission via UART0.

9.5.4 UARTEN Enable Register

9EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UARTEN	OUTSEL		OUTEN	FLH24MOUTEN	-	-	UART1EN	UART0EN
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	OUTSEL	11: XTH output 10: System clock output 01: RCL38K clock output 00: RCH16M clock output
5	OUTEN	CLK output enable: 1: CLKOUT output enabled 0: CLKOUT output disabled Note: After enabling the output, P0_3 functions as the CLKOUT pin to output the clock signal.
4	FLH24MOUTEN	-
3:2	-	-
1	UART1EN	UART1 enable bit: 0: P1.4 and P1.5 function as GPIO. 1: P1.4 and P1.5 function as RX1 and TX1 for UART1. Note: This bit is not required to be set when P1_1 and P1_0 function as TX1 and RX1 for UART1.

0	UART0EN	UART0 enable bit: 0: P2.6 and P2.7 function as GPIO. 1: P2.6 and P2.7 function as TX0 and RX0 for UART0. Note: This bit is not required to be set when P1_3 and P1_2 function as TX0 and RX0 for UART0.

9.6 UART1 Register Description

Table 9-4: List of Registers

Address	Name	Description
9BH	UART1_S1CON	Interrupt register
9DH	UART1_S1RELL	Baud rate configuration register
BBH	UART1_S1RELH	Baud rate configuration register
9CH	UART1_S1BUF	Data register
9EH	UARTEN	Enable register

9.6.1 UART1_S1CON Interrupt Register

9BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART1_S1CON	SM	-	SM21	REN1	TB81	RB81	TI1	RI1
R/W	R/W	-	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	SM	UART1 mode selection bit: SM=0, Mode A, 9-bit UART, Baud Rate: Configurable SM=1, Mode B, 8-bit UART, Configurable
6	-	-
5	SM21	UART1 multi-machine communication enable bit: 0: Disable the multi-machine communication. 1: Enable the multi-machine communication to receive only 9-bit data with RB81 = 1.
4	REN1	UART1 receive enable bit: 0: Disable data reception on UART1. 1: Enable data reception on UART1.

3	TB81	The 9th transmit data bit of UART1
2	RB81	The 9th receive data bit of UART1
1	TI1	UART1 transmit interrupt flag bit: Upon completion of data transmission, this bit shall be set by hardware and must be cleared by software.
0	RI1	UART1 receive interrupt flag bit: Upon completion of data reception, this bit shall be set by hardware and must be cleared by software.

9.6.2 UART1_S1REL Baud Rate Configuration Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART1_S1RELL (9DH)	S1RELL.7	S1RELL.6	S1RELL.5	S1RELL.4	S1RELL.3	S1RELL.2	S1RELL.1	S1RELL.0
Reset Value	1	1	1	0	0	1	1	0
UART1_S1RELH (BBH)	-	-	-	-	-	-	S1RELH.1	S1RELH.0
Reset Value	-	-	-	-	-	-	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit No.	Bit Designator	Description
7:0 1:0	S1RELL[7:0] S1REH[1:0]	UART0 baud rate configuration register: S1RELH + S1RELL constitute the baud rate setting S1REL[9:0] Baud rate = $\frac{\text{SYSCK}}{16\times(1024-\text{S1REL})}$

9.6.3 UART1_S1BUF Data Register

9CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART1_S1BUF	S1BUF.7	S1BUF.6	S1BUF.5	S1BUF.4	S1BUF.3	S1BUF.2	S1BUF.1	S1BUF.0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	S1BUF[7:0]	UART1 data register: Reading S1BUF returns the data received by UART1. Writing to S1BUF initiates data transmission via UART1.

9.6.4 UARTEN Enable Register

Please refer to Chapter "UARTEN Enable Register" for details.

9.7 Baud Rate

- UART0 Mode 1 and Mode 3

  Baud rate = $\frac{\text{SYSCK}}{16\times(1024-\text{S0REL})}$

- UART1

  Baud rate = $\frac{\text{SYSCK}}{16\times(1024-\text{S1REL})}$

When SYSCLK is 16 MHz, the configuration values of common baud rates SxREL and the actual errors are shown in the following table:

Table 9-5: Table of Baud Rate Error

Target Baud Rate	SxREL	Actual Baud Rate	Error
115200	1015	111111	3.5%
57600	1007	58824	-2.1%
38400	998	38462	-0.2%
19200	972	19231	-0.2%
9600	920	9615	-0.2%
4800	816	4808	-0.16%
2400	607	2398	0.08%

10 UART2/3 (Universal Asynchronous Receiver Transmitter)

The universal asynchronous receiver/transmitter (hereinafter referred to as UART) is a widely used serial communication interface that supports full duplex communication. The UART converts parallel data from memory or a processor into serial data for transmission to the UART receiver of an external device, or converts serial data received from the UART external device into parallel data for the processor. UART supports serial communication with external interface devices.

10.1 Main Features

Functional features:

- Providing standard asynchronous communication bits (start bit, parity bit, and stop bit):
  - Generating 1 start bit
  - Generating 1 parity bit (odd or even), or no parity bit
  - Generating 1 stop bit
  - Data bytes are transmitted from LSB to MSB
- 8-bit 4-level RX FIFO
- Programmable baud rate (adjustable according to parameters F/D)
- Supporting data communication and error handling interrupts:
  - Status bit can be accessed by either polling or interrupt.

- FIFO flags: not empty, half-full, full, and overflow
- Parity error flag

- Start bit validity detection function
- 2 × 8-bit baud rate parameter registers
- Supporting transfer at common baud rates such as 9600 bps, 19200 bps and 115200 bps

10.2 Register Description

UART2 register base address: 0xCD00; UART3 register base address: 0xCE00.

Table 10-1: List of Registers

Offset	Name	Description
0x00	UART_ISR	UART interrupt status register
0x01	UART_IER	UART interrupt enable register
0x02	UART_CR	UART control register
0x03	UART_TDR	UART transmit data register
0x03	UART_RDR	UART receive data register
0x04	UART_BPR_L	UART baud rate parameter low register
0x05	UART_BPR_H	UART baud rate parameter high register

10.2.1 UART_ISR Interrupt Status Register

CD00H/CE00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_ISR	RSV		FIFO_NE	FIFO_HF	FIFO_FU	FIFO_OV	TXEND	TRE
R/W	R		R/W	R/W	R/W	R	R/W	R
Reset Value	0		0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	RSV	Reserved
5	FIFO_NE	FIFO not empty flag: When FIFO_NE = 0, FIFO is empty. When FIFO_NE = 1, FIFO is not empty. This bit is automatically cleared when FIFO is read empty. It can also be cleared by software writing 0.

4	FIFO_HF	FIFO half-full flag: When FIFO_HF = 0, FIFO is not half-full. When FIFO_HF = 1, FIFO is half-full. This bit is automatically cleared when data in the FIFO is read. It can also be cleared by software writing 0.
3	FIFO_FU	FIFO full flag: When FIFO_FU = 0, FIFO is not full. When FIFO_FU = 1, FIFO is full. This bit is automatically cleared when data in the FIFO is read. It can also be cleared by software writing 0.
2	FIFO_OV	RX FIFO receive overflow error: When FIFO_OV = 0, no receive overflow error has occurred. When FIFO_OV = 1, a receive overflow error has occurred. This bit can be cleared by software writing 0.
1	TXEND	UART transmission complete flag: When TXEND = 0, the transmission is not completed. When TXEND = 1, the transmission is completed. This bit is set to 1 by hardware, and cleared by software via writing 0.
0	TRE	UART transmit/receive parity error flag: When TRE = 0, no parity error occurs upon completion of UART transmission/reception. When TRE = 1, a parity error occurs upon completion of UART transmission/reception. This bit is set to 1 by hardware, and cleared by software via writing 0.

10.2.2 UART_IER Interrupt Enable Register

CD01H/CE01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_IER	RSV		FIFO_EN	FIFO_HFEn	FIFO_FUEn	FIFO_OVEn	TXENDEn	TREEn
R/W	R		R/W	R/W	R/W	R/W	R/W	R
Reset Value	0		0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	RSV	Reserved
5	FIFO_EN	FIFO not empty interrupt enable: 0: Disabled 1: Enabled

4	FIFO_HFEn	FIFO half-full interrupt enable: 0: Disabled 1: Enabled
3	FIFO_FUEn	FIFO full interrupt enable: 0: Disabled 1: Enabled
2	FIFO_OVEn	RX FIFO receive overflow interrupt enable: 0: Disabled 1: Enabled
1	TXENDEn	UART transmission complete interrupt enable: 0: Disabled 1: Enabled
0	TREEn	UART transmit/receive parity error interrupt enable: 0: Disabled 1: Enabled

10.2.3 UART_CR Control Register

CD02H/CE02H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_CR	RSV	TX_EN	TX_OEN	UART_LB	UART_P0	FLUSH	TRS	ODD_EN
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:5	RSV	Reserved
6	TX_EN	UART single-wire mode enable: 0: Disabled 1: Enabled
5	TX_OEN	UART TX pin data transfer direction control in single-wire mode: 0: TX pin as data output 1: TX pin as data input
4	UART_LB	UART loopback test mode enable: 0: Disabled 1: Enabled
3	UART_P0	Parity check enable: 0: Enabled 1: Disabled

2	FLUSH	Clear data and pointer in UART RX FIFO: 0: Do not clear 1: Clear
1	TRS	UART data transmission flag: 0: Data transmission disabled 1: Data transmission enabled
0	ODD_EN	Parity mode selection: 0: Even parity 1: Odd parity

10.2.4 UART_TDR Transmit Data Register

CD03H/CE03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_TDR	UARTDATA							
R/W	W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	UARTDATA	Store the data to be transmitted.

10.2.5 UART_RDR Receive Data Register

CD03H/CE03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_RDR	UARTDATA							
R/W	R							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	UARTDATA	Store the data to be received.

10.2.6 UART_BPR_L Baud Rate Parameter Low Register

CD04H/CE04H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_BPR_L	UART_BPR_L							
R/W	R/W							
Reset Value	0x74							

Bit No.	Bit Designator	Description
7:0	UART_BPR_L	The baud rate parameter registers UART_BPR_H and UART_BPR_L constitute a 16-bit frequency divider. **For example, if the system clock is 40 MHz and a baud rate of 9600 is desired,** then UART_BPR = 40 × 1000000 ÷ 9600 = 1046H, i.e., UART_BPR_H = 10H and UART_BPR_L = 46H. **For example, if the system clock is 40 MHz and a baud rate of 19200 is desired,** then UART_BPR = 0823H, i.e., UART_BPR_H = 08H and UART_BPR_L = 23H.

Note: The system clock shall be with more than 12 times the baud rate.

10.2.7 UART_BPR_H Baud Rate Parameter High Register

CD05H/CE05H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
UART_BPR_H	UART_BPR_H							
R/W	R/W							
Reset Value	0x01							

Bit No.	Bit Designator	Description
7:0	UART_BPR_H	The baud rate parameter registers UART_BPR_H and UART_BPR_L constitute a 16-bit frequency divider. **For example, if the system clock is 40 MHz and a baud rate of 9600 is desired,** then UART_BPR = 40 × 1000000 ÷ 9600 = 1046H, i.e., UART_BPR_H = 10H, UART_BPR_L = 46H. **For example, if the system clock is 40 MHz and a baud rate of 19200 is desired,** then UART_BPR = 0823H, i.e., UART_BPR_H = 08H, UART_BPR_L = 23H.

Note: The system clock must be more than 12 times the baud rate.

10.3 Process Description

10.3.1 UART Transmission Process

1. Configure PCLK1 and PRESET1 to enable UART and release the reset.

2. Multiplex IO into UART_RX and UART_TX according to the IO multiplexing relation.
3. Configure UART_CR to set whether parity is enabled and enable data transmission.
4. Configure UART_BPR_H and UART_BPR_L to set the baud rate based on calculations.
5. Enable UART interrupts and global interrupts, configure UART_IER to enable transmission completion interrupt.
6. Write data to UART_TDR.
7. Query the interrupt status in UART_ISR.
8. Transmission is complete.

10.3.2 UART Reception Process

1. Configure PCLK1 and PRESET1 to enable UART and reset release.
2. Multiplex IO into UART_RX and UART_TX according to the IO multiplexing relation.
3. Configure UART_CR, set whether there is parity, and enable data transmission.
4. Configure UART_BPR_H and UART_BPR_L to set the baud rate based on calculations.
5. Enable UART interrupts and global interrupts, configure UART_IER to enable RX FIFO not empty interrupt.
6. Query the interrupt status in UART_ISR.
7. Read data from UART_TDR.
8. Transmission is complete.

Note: For serial port I/O, the internal pull-up of the corresponding IO must be enabled in the PxPUN register; otherwise, the RX pin will be in a floating state and susceptible to interference.

11 SPI

11.1 Overview

The serial peripheral interface (SPI) is a serial synchronous communication means for external devices to exchange data via a single line. The chip provides an SPI module that can be configured as either a master or a slave device to realize SPI communication with external devices.

11.2 Main Features

- Supporting standard SPI protocol, with configurable master and slave modes
- Supporting MISO, MOSI, single-line transmission, half-duplex and full-duplex transmission, and configurable data endianness (big-endian or little-endian)
- Programmable clock polarity and phase
- Supporting TX_ONLY mode transmission
- Supporting PCB board delay compensation, and combinational logic filtering for SSN/SCK/MOSI input signals in slave mode

11.3 Register Description

SPI register base address: 0xC400

Table 11-1: List of Registers

Address	Name	Description
0xC400	SPI_CR1	Control register 1
0xC401	SPI_CR2	Control register 2

Address	Name	Description
0xC402	SPI_CR3	Control register 3
0xC403	SPI_CR4	Control register 4
0xC404	SPI_IE	Interrupt enable register
0xC405	SPI_SR	Status register
0xC406	SPI_TXBUF	Transmit buffer register
0xC407	SPI_RXBUF	Receive buffer register

11.3.1 SPI_CR1 Control Register

C400H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_CR1	BR[2:0]			SSN_MODE	LSBFIRST	MSTR	CPOL	CPHA
R/W	R/W			R/W	R/W	R/W	R/W	R/W
Reset Value	1			0	0	1	0	0

Bit No.	Bit Designator	Description
7:5	BR[2:0]	Baud rate configuration bits in master mode: 000: $f_{PCLK}/2$ 001: $f_{PCLK}/4$ 010: $f_{PCLK}/8$ 011: $f_{PCLK}/16$ 100: $f_{PCLK}/32$ 101: $f_{PCLK}/64$ 110: $f_{PCLK}/128$ 111: $f_{PCLK}/256$ These bits cannot be modified while communication is in progress.
4	SSN_MODE	In Master mode, SSN_MODE indicates whether SSN will be pulled high after every 8 bits are transmitted. 0: When TXBUF is not empty and 8 bits have been transmitted completely, if WAIT_CNT is not 0, SSN will be pulled high after waiting for (1 + WAIT_CNT) SCK cycles. 1: When TXBUF is not empty and 8 bits have been transmitted completely, SSN will be pulled high.
3	LSBFIRST	Frame format: 0: MSB first (bit7) 1: LSB first (bit0) Note: This bit cannot be modified while communication is in progress.

2	MSTR	Master/slave mode selection: 0: Slave mode 1: Master mode
1	CPOL	Clock polarity selection: 0: Serial clock stops at low level. 1: Serial clock stops at high level. Note: This bit cannot be modified while communication is in progress.
0	CPHA	Clock phase selection: 0: The first clock edge is the first capture edge. 1: The second clock edge is the first capture edge. Note: This bit cannot be modified while communication is in progress.

Note:

- When an error occurs, this register remains unchanged. To restart SPI, the software shall first write SPI_en to 0 and then to 1.
- After changing CPOL and CPHA, SPI shall be restarted, and the software shall first write SPI_en to 0 and then to 1.

11.3.2 SPI_CR2 Control Register

C401H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_CR2	SAMPLE_P	TXONLY_AUTO_CLR	SPI_EN	SSN_MCU_EN	WAIT_CNT		RSV	RSV
R/W	R/W	R/W	R/W	R/W	R/W		R	R
Reset Value	0	1	0	0	0		0	0

Bit No.	Bit Designator	Description
7	SAMPLE_P Sdin_sample_mode	Master mode: sampling position for MISO signal from slave 0: The sampling position complies with the protocol. 1: When the baud rate is lower than $f_{PCLK}/2$, the sampling position is delayed by at least one SPICLK cycle (specifically, delayed by half an SPI SCK cycle). Note: This bit does not take effect when the baud rate is $f_{PCLK}/2$.

6	TXONLY_AUTO_CLR (original TXONLY_EN)	TXONLY hardware auto-clear enable: 0: Disable TXONLY hardware auto-clear. 1: Enable TXONLY hardware auto-clear. After the software sets TXONLY in SPI_CR3, the hardware automatically clears it upon completion of the transmission.
5	SPI_EN	SPI enable: SPI is enabled/disabled by controlling the peripheral clock: 0: Disable SPI. Enter the reset state, and clear TXBUF and RXBUF. 1: Enable SPI.
4	SSN_MCU_EN	Software control of SSN port in master mode: 1: SSN is controlled by software, and the enable is effective. 0: SSN is controlled by internal hardware.
3:2	WAIT_CNT	Wait cycles between 8-bit transfers in master mode: 00: No wait 01: Insert 2 SCK cycles of wait. 10: Insert 3 SCK cycles of wait. 11: Insert 4 SCK cycles of wait.
1:0	RSV	Reserved

Note: When an error occurs, this register remains unchanged. To restart SPI, the software shall first write SPI_en to 0 and then to 1.

11.3.3 SPI_CR3 Control Register

C402H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_CR3	SCK_EN	MOSI_EN	MISO_EN	CS_EN	TX_ONLY	SSN_MCU	Signal_filter	send_p
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	0	1	1	0

Bit No.	Bit Designator	Description
7	SCK_EN	P1_3 is enabled as the SPI_SCK signal. When this bit is 1 and SPI_EN is 1, P1_3 functions as the SPI_SCK signal. Note: This bit is not required to be set when P0_1/P0_4/P2_3 are configured as SPI_SCK.

6	MOSI_EN	P1_4 is enabled as the SPI_MOSI signal. When this bit is 1 and SPI_EN is 1, P1_4 functions as the SPI_MOSI signal. Note: This bit is not required to be set when P2_0/P2_3/P2_7 are configured as SPI_MOSI.
5	MISO_EN	P1_5 is enabled as the SPI_MISO signal. When this bit is 1 and SPI_EN is 1, P1_5 functions as the SPI_MISO signal. Note: This bit is not required to be set when P1_1/P2_2/P2_6 are configured as SPI_MISO.
4	CS_EN	P0_3 is enabled as the SPI_CSN signal. When this bit is 1 and SPI_EN is 1, P0_3 functions as the SPI_CSN signal. Note: This bit is not required to be set when P0_0/P2_2/P2_5 are configured as SPI_CSN.
3	TX_ONLY	Enable of TX_ONLY for SPI: 0: Disable TX_ONLY mode 1: Enable TX_ONLY mode
2	SSN_MCU	In Master mode, if SSN_MCU_EN = 1, MCU can control the SSN output port by writing to this bit: 0: SSN is written to 0 by software. 1: SSN is written to 1 by software.
1	Signal_filter	Whether to digitally filter possible glitches on SSN/SCK/MOSI: 0: No filtering 1: Filtering enabled
0	send_p Sdout_send_mode	In Slave mode, the transmit start point clock is used for the MOSI signal output by the slave: 0: Transmit according to the protocol-specified clock point. 1: Transmit half a cycle in advance

Note: When an error occurs, this register remains unchanged. To restart SPI, the software shall first write SPI_en to 0 and then to 1.

11.3.4 SPI_CR4 Control Register

C403H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_CR4	RSV	RSV	RSV	RSV	CLR_ TXBUF	CLR_RXBUF	RSV	RSV
R/W	R	R	R	R	W	W	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:4	RSV	Reserved
3	CLR_TXBUF	Writing 1 clears all the contents of TX_BUF and the TXBUF_EMPTY flag bit, which is automatically reset to 0 by hardware.
2	CLR_RXBUF	Writing 1 clears all the contents of RX_BUF and the RXBUF_FULL flag bit, which is automatically reset to 0 by hardware.
1:0	RSV	Reserved

Note: When an error occurs, the TXONLY bit will be automatically reset to 0 by hardware. Therefore, this register shall be reconfigured when restarting SPI.

11.3.5 SPI_IE Interrupt Enable Register

Interrupts are generated based on the enable settings in this interrupt enable register:

C404H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_IE	RSV	RSV	RSV	RSV	RSV	ERROR_IE	TX_E_IE	RX_NE_IE
R/W	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:3	RSV	Reserved
2	ERROR_IE	Error interrupt enable (including TXBUF/RXBUF overflow, master/slave error): 0: Disable the interrupt. 1: Enable the interrupt.
1	TX_E_IE	TXBUF empty interrupt enable: 0: Disable the interrupt. 1: Enable the interrupt.
0	RX_NE_IE	RXBUF not empty interrupt enable: 0: Disable the interrupt. 1: Enable the interrupt.

11.3.6 SPI_SR Status Register

C405H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_SR	RSV	RSV	RSV	RXBUF_WCOL	TXBUF_WCOL	BUSY	TXBUF_EMPTY	RXBUF_FULL
R/W	R	R	R	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	0

Bit No.	Bit Designator	Description
7:5	RSV	Reserved
4	RXBUF_WCOL	RX overflow, cleared to 0 by software writing 0.
3	TXBUF_WCOL	When the TXBUF is full and the MCU attempts to write to the TXBUF: 1: Conflict 0: No conflict This bit is cleared to 0 by software writing 0.
2	BUSY	Indication: 0: TXBUF is empty and SPI is not transmitting data. 1: TXBUF is not empty, or SPI is transmitting data. In slave mode, based on SSN and TXBUF, if SSN is high and TXBUF is empty, the BUSY signal is 0.
1	TXBUF_EMPTY	Writing to TXBUF clears this flag bit: 0: There is data in TXBUF waiting to be transmitted. 1: There is no data in TXBUF, and new data can be written.
0	RXBUF_FULL	Reading RXBUF clears this flag bit: 0: There is no data in RXBUF. 1: There is data in RXBUF.

11.3.7 SPI_TXBUF Transmit Data Register

The MCU writes the data to be transmitted to this register to buffer the transmit data into SPI_TXBUF. SPI_TXBUF has no physical register and only supports write operations.

C406H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_TXBUF	WR_DATA							
R/W	W							
Reset Value	0							

Bit No.	**Bit Designator**	**Description**
7:0	WR_DATA	When writing to this register, if the SPI_TXBUF is already full, an overflow interrupt will be generated.

11.3.8 SPI_RXBUF Receive Buffer Register

Data received via the SPI interface is first buffered in SPI_RXBUF. After the SPI interface completes the reception of one byte, it will write one byte of data into SPI_RXBUF. The MCU can obtain the data received from the SPI interface by reading this register.

C407H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SPI_RXBUF	D7:D0							
R/W	R							
Reset Value	0							

Bit No.	**Bit Designator**	**Description**
7:0	D7:D0	The MCU performs a read operation on this address based on the non-empty interrupt of SPI_RXBUF to read the data in the internal SPI_RXBUF.

11.4 Software Operation Process

11.4.1 Master Transmission

1. Configure the SPI 4-wire pin alternate function (via relevant bits in SPI_CR3 register or IO_CFG register).
2. Write the MSTR bit in the SPI_CR1 register to enable master mode.
3. If software control of the SSN signal is required, write the SSN_MCU_EN bit in the SPI_CR2 register.
4. Write the BR bit in the SPI_CR1 register to configure the SPI communication baud rate.

5. Write the CPOL and CPHA bits in the SPI_CR1 register to configure the SPI communication mode.
6. If interrupts are used, write the EAL and ESPI bits and write the SPI_IE register to enable the TX_E_IE interrupt.
7. Write the SPI_SR register to clear all interrupt flags. Write the SPI_CR4 register to clear the contents of TX_BUF.
8. Write the SPI_EN bit in the SPI_CR2 register to enable SPI.
9. Write 0 to the SSN_MCU bit in the SPI_CR3 register to start SPI communication.
10. Wait for the TXBUF_EMPTY bit in the SPI_SR register to be 1, then place the data to be transmitted to the slave into the SPI_TXBUF register.
11. If multiple bytes of data need to be transmitted, repeat step 10. After transmitting all the data, wait for the BUSY bit in the SPI_SR register to change from 1 to 0, then end the transmission.
12. Write 1 to the SSN_MCU bit in the SPI_CR3 register to end SPI communication.

11.4.2 Master Reception

1. Configure the SPI 4-wire pin alternate function (via relevant bits in SPI_CR3 register or IO_CFG register).
2. Write the MSTR bit in the SPI_CR1 register to enable master mode.
3. If software control of the SSN signal is required, write the SSN_MCU_EN bit in the SPI_CR2 register.
4. Write the BR bit in the SPI_CR1 register to configure the SPI communication baud rate.
5. Write the CPOL and CPHA bits in the SPI_CR1 register to configure the SPI communication

mode.

6. Write the EAL and ESPI bits, then write the SPI_IE register to enable the RX_NE_IE interrupt.
7. Write the SPI_SR register to clear all interrupt flags. Write the SPI_CR4 register to clear the contents of TX_BUF.
8. Write the SPI_EN bit in the SPI_CR2 register to enable SPI.
9. Write 0 to the SSN_MCU bit in the SPI_CR3 register to start SPI communication.
10. Wait for the TXBUF_EMPTY bit in the SPI_SR register to be 1, then place 1 byte of data to be transmitted to the slave in the SPI_TXBUF register. Afterwards, wait for the RX_BUF not empty interrupt to be triggered, read the RXBUF register, and receive the data transmitted from the slave.
11. If multiple bytes of data need to be received, repeat step 10. After receiving all the data, wait for the BUSY bit in the SPI_SR register to change from 1 to 0, then end the transmission.
12. Write 1 to the SSN_MCU bit in the SPI_CR3 register to end SPI communication.

11.4.3 Slave Transmission

1. Configure the SPI 4-wire pin alternate function (via relevant bits in SPI_CR3 register or IO_CFG register).
2. Write the MSTR bit in the SPI_CR1 register to enable slave mode.
3. Write the CPOL and CPHA bits in the SPI_CR1 register to configure the SPI communication mode.
4. If interrupts are used, write the EAL and ESPI bits and write the SPI_IE register to enable the TX_E_IE interrupt.
5. Write the SPI_SR register to clear all interrupt flags. Write the SPI_CR4 register to clear the

contents of TX_BUF.

6. Write the SPI_EN bit in the SPI_CR2 register to enable SPI.
7. Set the TX_ONLY bit in the SPI_CR3 register to enable transmit-only mode.
8. Wait for the TX_E_IE interrupt to trigger, or after polling to confirm that the TXBUF_EMPTY status bit in the SPI_SR register is set, then write the data to be transmitted into the RXBUF register, poll the BUSY bit in the SPI_SR register, and wait for the TXBUF to become empty.
9. If the slave needs to transmit multiple pieces of data, repeat Step 8.

11.4.4 Slave Reception

1. Configure the SPI 4-wire pin alternate function (via relevant bits in SPI_CR3 register or IO_CFG register).
2. Write the MSTR bit in the SPI_CR1 register to enable slave mode.
3. Write the CPOL and CPHA bits in the SPI_CR1 register to configure the SPI communication mode.
4. If interrupts are used, write the EAL and ESPI bits and write the SPI_IE register to enable the RX_NE_IE interrupt.
5. Write the SPI_SR register to clear all interrupt flags. Write the SPI_CR4 register to clear the contents of TX_BUF.
6. Write the SPI_EN bit in the SPI_CR2 register to enable SPI.
7. Wait for the RX_NE_IE interrupt to trigger, or after polling to confirm that the RXBUF_FULL status bit in the SPI_SR register is set, then read the data in the RXBUF register.

12 LPTIMER (Low-power Timer)

12.1 Overview

LPTIMER is a 16-bit low-power timer/counter module operating in the Always-on power domain. By selecting an appropriate operating clock, LPTIMER can remain operational in various low-power modes with extremely low power consumption. Given its capability to run even with no internal clock source, LPTIMER can be used as a pulse counter in low-power mode. Also, in combination with an external input trigger signal, LPTIMER is able to realize timeout function regarding waking up the system from low-power modes.

12.2 Main Features

- 16-bit upcounter
- 3-bit asynchronous clock prescaler with 8 division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable operating clocks:

  Internal clock sources: LSCLK, RCLP, system clock

  External clock source: LPTIN (with analog filtering)
- 16-bit compare register
- 16-bit target value register
- Software/hardware trigger
- Two input captures
- Input polarity selection
- External pulse counting without clock
- Sleep timeout wake-up triggered externally
- 2-channel 16-bit PWM

12.3 Structure Diagram

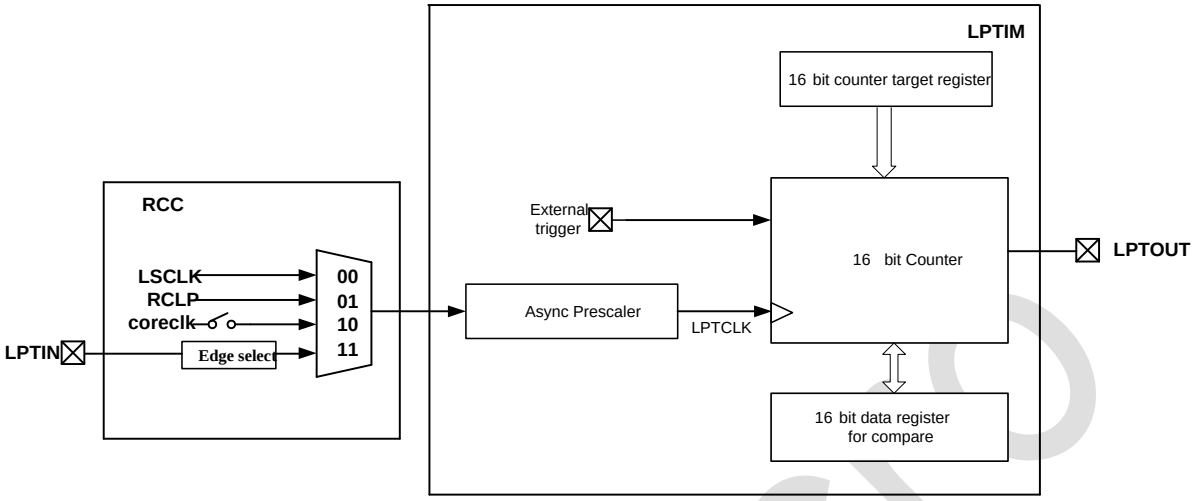


Figure 12-1: Structure Diagram

12.4 Operating Modes

12.4.1 General-purpose Timer

- Operates using an internal clock or external input clock
- There is a synchronization process of two counting clocks after enabling.
- Starts working immediately upon enabling, no trigger required

12.4.2 Trigger Pulse Counting

- Operates using an internal clock
- The internal clock samples the asynchronous trigger signal from the external input.
- It can count on the rising edge, falling edge, or both edges of the trigger signal.
- There is a synchronization process of two counting clocks after enabling.

12.4.3 External Asynchronous Pulse Counting

- The external input pulse is directly used as the counting clock
- The input polarity is configurable to implement rising-edge or falling-edge counting.
- No trigger is required.
- There is no synchronization process after enabling.

12.4.4 Timeout Mode

- Operates using an internal clock or external input clock
- It samples the asynchronous trigger signal from the external input.
- The first trigger starts the counter, and subsequent triggers will reset and restart the counter.
- If no new trigger occurs before the counter overflows, an overflow interrupt is generated, the counting stops, and the enable is cleared.
- There is a synchronization process of two counting clocks when enabled.

12.4.5 Counting Mode

There are two counting modes for LPTIMER.

- Continuous counting mode: The counter keeps running after being triggered until it is disabled. When the counter reaches the target value, it returns to 0 and restarts counting, generating an overflow interrupt.
- Single-shot counting mode: The counter counts to the target value after being triggered, then resets to 0 and stops automatically, generating an overflow interrupt.

12.4.6 Externally Triggered Timeout Wakeup

LPTIMER can be enabled by an external trigger signal or by software. In timeout mode, the first valid edge of the external trigger input starts the counter, and subsequent trigger signals clear the counter. If there is no valid trigger signal before the counter reaches the compare value, a timeout interrupt is generated to wake up MCU.

The valid edge of the external trigger signal can be configured by a register. The external trigger signal is considered an asynchronous input, so there is a latency of at least two counting clocks for sampling and determining the valid edge.

12.4.7 16-bit PWM

LPTIMER starts counting from 0x0000 once the PWM mode is enabled. The output goes high when the count value equals the compare value while goes low when the count value equals the final value. The PWM period is determined by the final value register, and the duty cycle is determined by the compare value register.

12.5 Register Description

LPTIMER register base address: 0xC800

Table 12-1: List of Registers

Address	Name	Description
0xC800	LPTIMER_CFG0	LPTIMER configuration register 0
0xC801	LPTIMER_CFG1	LPTIMER configuration register 1
0xC802	LPTIMER_CNT_L	LPTIMER count value low register
0xC803	LPTIMER_CNT_H	LPTIMER count value high register
0xC804	LPTIMER_CMP1_L	LPTIMER capture/compare value 1 low register
0xC805	LPTIMER_CMP1_H	LPTIMER capture/compare value 1 high register
0xC806	LPTIMER_TARGET_L	LPTIMER target value low register

Address	Name	Description
0xC807	LPTIMER_TARGET_H	LPTIMER target value high register
0xC808	LPTIMER_IE	LPTIMER interrupt enable register
0xC809	LPTIMER_IF	LPTIMER interrupt flag register
0xC80A	LPTIMER_CTRL	LPTIMER control register
0xC80B	LPTIMER_CCMCFG1	LPTIMER capture channel 1 control register
0xC80C	LPTIMER_CCMCFG2	LPTIMER capture channel 2 control register
0xC80D	LPTIMER_CMP2_L	LPTIMER capture/compare value 2 low register
0xC80E	LPTIMER_CMP2_H	LPTIMER capture/compare value 2 high register
0xC811	LPTIMER_LOAD	Auto-load register
0xC812	LPTIMER_BUFFER_L	Count value load low register
0xC813	LPTIMER_BUFFER_H	Count value load high register

12.5.1 LPTIMER_CFG0 Register

C800H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CFG0	TRIGCFG		EDGESEL	CLKSEL		DIVSEL		
R/W	R/W		R/W	R/W		R/W		
Reset Value	0		0	1	0	0		

Bit No.	Bit Designator	Description
7:6	TRIGCFG	External trigger edge selection: 00: Trigger on rising edge of external input signal 01: Trigger on falling edge of external input signal 10/11: Trigger on both rising and falling edges of external input signal These bits cannot be modified while communication is in progress.
5	EDGESEL	LPTIN input edge selection: 0: Count on rising edge of LPTIN 1: Count on falling edge of LPTIN
4:3	CLKSEL	Clock source selection: 00: LSCLK as counting clock (38kHz RCL) 01: RCLP as counting clock (1Hz clock divided from 38kHz RCL) 10: Gated PCLK as counting clock 11: LPTIN as counting clock
2:0	DIVSEL	Counter clock prescaler selection: 000: Divided by 1

		001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110: Divided by 64 111: Divided by 128

12.5.2 LPTIMER_CFG1 Register

C801H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CFG1	EXTRIGGER_IO_IEN	LPOUT_IO_IEN	LPTIN_IO_IEN	TMODE		MODE	PWM	POLARITY
R/W	R/W	R/W	R/W	R/W		R/W	R/W	R/W
Reset Value	0	0	0	0		0	0	0

Bit No.	Bit Designator	Description
7	EXTRIGGER_IO_IEN	1: Set P1_1 as EXTRIGGER_IO_IEN Note: This bit is not required to be set when P1_4 is used as EXTRIGGER_IO.
6	LPOUT_IO_IEN	1: Set P0_3 as LPOUT1 Note: This bit is not required to be set when P0_0/P2_0 is used as LPTOUT1.
5	LPTIN_IO_IEN	1: Set P1_0 as LPTIN Note: This bit is not required to be set when P1_3 is used as LPTIN.
4:3	TMODE	Operating mode selection: 00: General-purpose timer mode with waveform output 01: Pulse-trigger counting mode 10: External asynchronous pulse counting mode 11: Timeout mode
2	MODE	Counting mode: 0: Continuous counting mode: The counter keeps running after being triggered until it is disabled. When the counter reaches the target value, it returns to 0 and restarts counting, generating an overflow interrupt. 1: Single-shot counting mode: The counter counts to the target value after being triggered, then resets to 0 and stops

		automatically, generating an overflow interrupt.
1	PWM	Pulse width modulation (PWM) mode: 0: Periodic square wave output 1: PWM output mode
0	POLARITY	Counter clock prescaler selection: 0: Positive polarity waveform, i.e., the output waveform rises when the count value equals the compare value for the first time. 1: Negative polarity waveform, i.e., the output waveform falls when the count value equals the compare value for the first time.

12.5.3 LPTIMER_CNT Count Value Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CNT_L (C802H)	CNT16[7:0]							
LPTIMER_CNT_H (C803H)	CNT16[15:8]							
R/W	R							
Reset Value	0							

Bit No.	Bit Designator	Description
15:0	CNT16	Count value

12.5.4 LPTIMER_CMP1 Compare Value Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CMP1_L (C804H)	COMPARE_REG[7:0]							
LPTIMER_CMP1_H (C805H)	COMPARE_REG[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
15:0	COMPARE_REG	Capture/compare value register 1: Reading the LPTIMER_CMP1_H register will clear the COMPIF flag bit.

12.5.5 LPTM_TARGET Target Value Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_TARGET_L (C806H)	TARGET_REG[7:0]							
LPTIMER_TARGET_H (C807H)	TARGET_REG[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
15:0	TARGET_REG	Target value register

12.5.6 LPTIMER_IE Interrupt Enable Register

Interrupts are generated in the interrupt enable register based on the enable state of this register:

C808H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_IE	RSV				COMP2IE	TRIGIE	OVIE	COMPIE
R/W	R				R/W	R/W	R/W	R/W
Reset Value	0				0	0	0	0

Bit No.	Bit Designator	Description
7:4	RSV	Reserved
3	COMP2IE	Compare match 2 interrupt enable bit: 1: Interrupt enabled at match 2 of the counter value and the compare value 0: Interrupt disabled at match 2 of the counter value and the compare value
2	TRIGIE	External trigger arrival interrupt enable: 1: Enable interrupt on external trigger arrival 0: Disable interrupt on external trigger arrival
1	OVIE	Counter overflow interrupt enable: 1: Enable counter overflow interrupt 0: Disable counter overflow interrupt

0	COMPIE	Compare match 1 interrupt enable bit: 1: Interrupt enabled at match 1 of the counter value and the compare value 0: Interrupt disabled at match 1 of the counter value and the compare value

12.5.7 LPTIMER_IF Interrupt Flag Register

C809H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_IF	RSV				COMP2IF	TRIGIF	OVIF	COMPIF
R/W	R				R/W	R/W	R/W	R/W
Reset Value	0				0	0	0	0

Bit No.	Bit Designator	Description
7:4	RSV	Reserved
3	COMP2IF	Capture/compare match 2 interrupt enable bit (can be cleared by writing 1): 1: Interrupt generated at match 2 of the counter value and the compare value 0: No interrupt generated
2	TRIGIF	External trigger arrival interrupt enable bit (can be cleared by writing 1): 1: External trigger arrival interrupt generated 0: No interrupt generated
1	OVIF	Counter overflow interrupt enable bit (can be cleared by writing 1): 1: Counter overflow interrupt generated 0: No interrupt generated
0	COMPIF	Capture / compare match 1 interrupt enable bit (can be cleared by writing 1): 1: Interrupt generated at match 1 of the counter value and the compare value 0: No interrupt generated

12.5.8 LPTIMER_CTRL Control Register

C80AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CTRL	RSV						CAP1SRSEL	LPTEN
R/W	R						R/W	R/W
Reset Value	0						0	0

Bit No.	Bit Designator	Description
7:2	RSV	Reserved
1	CAP1SRSEL	Channel 1 capture signal source selection: 0: LPT_CAP1 input 1: RCLP (1Hz clock divided from the 38kHz RCL)
0	LPTEN	LPTIMER enable: 1: Enable counter counting 0: Disable counter counting

12.5.9 LPTIMER_CCMCFG1 Control Register

C80BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CCMCFG1	RSV		CAP1EDGE		RSV		CC1S	CC1E
R/W	R		R/W		R		R/W	R/W
Reset Value	0		0		0		0	0

Bit No.	Bit Designator	Description
7:6	RSV	Reserved
5:4	CAP1EDGE	Channel 1 capture edge selection: 00: Capture on rising edge 01: Capture on falling edge 10: Capture on both rising and falling edges 11: Undefined
3:2	-	-
1	CC1S	Channel 1 capture/compare selection: 0: Channel 1 is configured as output. 1: Channel 1 is configured as input.
0	CC1E	Channel 1 capture/compare enable: 0: Disable channel 1 capture/compare function. 1: Enable channel 1 capture/compare function.

12.5.10 LPTIMER_CCMCFG2 Control Register

C80CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CCMCFG2	RSV		CAP2EDGE		RSV	CC2P	CC2S	CC2E
R/W	R		R/W		R	R/W	R/W	R/W
Reset Value	0		0		0	0	0	0

Bit No.	Bit Designator	Description
7:6	RSV	Reserved
5:4	CAP2EDGE	Channel 2 capture edge selection: 00: Capture on rising edge 01: Capture on falling edge 10: Capture on both rising and falling edges 11: Undefined
3	RSV	Reserved
2	CC2P	Channel 2 output polarity selection: 0: Output low when CNT ≤ CCR2 and high when CNT > CCR2 1: Output high when CNT ≤ CCR2 and low when CNT > CCR2
1	CC2S	Channel 2 capture/compare selection: 0: Channel 2 is configured as output. 1: Channel 2 is configured as input.
0	CC2E	Channel 2 capture/compare enable: 0: Enable channel 2 capture/compare function. 1: Enable channel 2 capture/compare function.

12.5.11 LPTIMER_CMP2 Compare Value Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_CMP2_L (C80DH)	COMPARE2_REG[7:0]							
LPTIMER_CMP2_H (C80EH)	COMPARE2_REG[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
15:0	COMPARE2_REG	Capture/compare value register 2 Reading the LPTIMER_CMP2_H register clears the COMP2F flag bit.

12.5.12 LPTIMER_LOAD Auto-load Register

C811H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_LOAD	RSV							LPTEN
R/W	R							R/W
Reset Value	0							0

Bit No.	Bit Designator	Description
7:1	RSV	Reserved
0	LPTIMER_LOAD	When the software writes LPTIMER_LOAD = 1, the hardware loads the current count value into the buffer register.

12.5.13 LPTIMER_BUFFER Count Value Load Register

	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LPTIMER_BUFFER_L (C812H)	BUFFER[7:0]							
LPTIMER_BUFFER_H (C813H)	BUFFER[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
15:0	BUFFER	When the software writes the LPTIMER_LOAD register, the hardware loads the current count value into the buffer register.

12.6 Software Operation Process

1. Select the clock source, set the prescaler value, and configure the operating mode and counting mode.
2. Set the values of the high and low compare registers.
3. Set the values of the high and low target registers.
4. Enable the interrupt flag.
5. Enable the LPTEN bit to start the counter.

12.6.1 General-purpose Timer

1. Configure LPTIMER_CFG.CLKSEL to select the clock source.
2. Configure LPTIMER_CFG.DIV to set the prescaler value.
3. Configure LPTIMER_CFG.MODE to set the counting mode.
4. Configure LPTIMER_CFG.TMODE to select the general-purpose timer mode.
5. Set the value of the LPTIMER_TARGET target register.
6. Set the LPTIMER_IE interrupt register to enable the overflow interrupt.
7. Set the LPTIMER_CTRL.LPTEN bit to enable the counter.

12.6.2 PWM Output

1. Configure LPTIMER_CFG.CLKSEL to select the clock source.
2. Configure LPTIMER_CFG.DIV to set the prescaler value.
3. Configure LPTIMER_CFG.MODE to set the counting mode.

4. Configure LPTIMER_CFG.PWM to select the PWM output mode.
5. Configure LPTIMER_CFG.POLARITY to select the waveform polarity.
6. Configure LPTIMER_CFG.TMODE to select the general-purpose timer mode.
7. Set the value of the LPTIMER_CMP compare register.
8. Configure LPTIMER_CCMCFG to enable the corresponding channel compare output.
9. Set the value of the LPTIMER_TARGET target register.
10. Set the LPTIMER_IE interrupt register to enable interrupts.
11. Set the LPTIMER_CTRL.LPTEN bit to enable the counter.

12.6.3 Pulse-trigger Counting Mode

1. Configure LPTIMER_CFG.CLKSEL to select the clock source.
2. Configure LPTIMER_CFG.DIV to set the prescaler value.
3. Configure LPTIMER_CFG.MODE to set the counting mode.
4. Configure LPTIMER_CFG.TRIGCFG to set the external trigger edge.
5. Configure LPTIMER_CFG.TMODE to select the pulse-trigger counting mode.
6. Set the LPTIMER_IE.TRIGIE interrupt register to enable the external trigger interrupt.
7. Set the LPTIMER_CTRL.LPTEN bit to enable the counter.

12.6.4 External Asynchronous Pulse Counting Mode

1. Configure LPTIMER_CFG.CLKSEL to select the clock source.
2. Configure LPTIMER_CFG.DIV to set the prescaler value.
3. Configure LPTIMER_CFG.MODE to set the counting mode.

4. Configure LPTIMER_CFG.EDGESEL to set the LPTIN input edge.
5. Configure LPTIMER_CFG.TMODE to select the external asynchronous pulse counting mode.
6. Set the value of the LPTIMER_TARGET target register.
7. Set the LPTIMER_IE interrupt register to enable interrupts.
8. Set the LPTIMER_CTRL.LPTEN bit to enable the counter.

12.6.5 Timeout Mode

1. Configure LPTIMER_CFG.CLKSEL to select the clock source.
2. Configure LPTIMER_CFG.DIV to set the prescaler value.
3. Configure LPTIMER_CFG.MODE to set the counting mode.
4. Configure LPTIMER_CFG.TRIGCFG to set the external trigger edge.
5. Configure LPTIMER_CFG.TMODE to select the timeout mode.
6. Set the value of the LPTIMER_TARGET target register.
7. Set the LPTIMER_IE interrupt register to enable the overflow interrupt.
8. Set the LPTIMER_CTRL.LPTEN bit to enable the counter.

Note: If no new trigger occurs before the counter overflows, an overflow interrupt is generated, the counting stops, and the enable bit is cleared. To reuse the function, the interrupt must be enabled again.

12.6.6 Input Capture

1. Configure LPTIMER_CFG.CLKSEL to select the clock source.
2. Configure LPTIMER_CFG.DIV to set the prescaler value.

3. Configure LPTIMER_CFG.MODE to set the counting mode.
4. Configure LPTIMER_CFG.POLARITY to select the waveform polarity.
5. Configure LPTIMER_CFG.TMODE to select the general-purpose timer mode.
6. Configure LPTIMER_CCMCFG to enable the corresponding channel capture input.
7. Set the value of the LPTIMER_TARGET target register.
8. Set the LPTIMER_IE interrupt register to enable interrupts.
9. Set the LPTIMER_CTRL.LPTEN bit to enable the counter.
10. Read the value of the LPTIMER_CMP compare register in the capture interrupt to obtain the count value at the time of capture.

13 GTIMER

13.1 Main Features

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler supporting real-time adjustment of counting clock division
- Flexible selection of counting clock sources
- Channels available for input capture, output compare, PWM (edge-aligned or center-aligned mode), and single-pulse output
- Supporting cascading with other timers

13.2 Structure Diagram

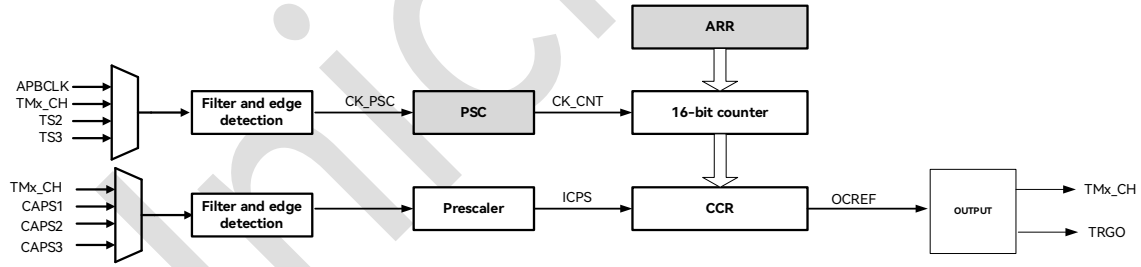


Figure 13-1: Structure Diagram

13.3 Register Description

- GTIMER0 register base address: 0xC900
- GTIMER1 register base address: 0xCA00
- GTIMER2 register base address: 0xCB00

Table 13-1: Register Description

Offset	Name	Description
0x00	GTIMER_CR0	GTIMER control register 0
0x01	GTIMER_CR1	GTIMER control register 1
0x02	GTIMER_CR2	GTIMER control register 2
0x03	GTIMER_CR3	GTIMER control register 3
0x04	GTIMER_IER	GTIMER interrupt enable register
0x05	GTIMER_SR	GTIMER status register
0x06	GTIMER_EGR	GTIMER event generation register
0x07	GTIMER_CCMR0	GTIMER capture/compare mode register 0
0x08	GTIMER_CCMR1	GTIMER capture/compare mode register 1
0x09	GTIMER_CCER	GTIMER capture/compare enable register
0x0A	GTIMER_CNT0	GTIMER counter register 0
0x0B	GTIMER_CNT1	GTIMER counter register 1
0x0C	GTIMER_PSC0	GTIMER prescaler register 0
0x0D	GTIMER_PSC1	GTIMER prescaler register 1
0x0E	GTIMER_ARR0	GTIMER auto-reload register 0
0x0F	GTIMER_ARR1	GTIMER auto-reload register 1
0x10	GTIMER_ARR2	GTIMER auto-reload register 2
0x11	GTIMER_ARR3	GTIMER auto-reload register 3
0x12	GTIMER_CCR0	GTIMER capture/compare register 0
0x13	GTIMER_CCR1	GTIMER capture/compare register 1
0x14	GTIMER_CCR2	GTIMER capture/compare register 2
0x15	GTIMER_CCR3	GTIMER capture/compare register 3

13.3.1 GTIMER_CR0 Control Register

C900H/CA00H/CB00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CR0	MMS	ARPE	CMS		CEN_ALL_EN	DIR	OPM	CEN
R/W	R/W	R/W	R/W		R/W	R/W	R/W	R/W
Reset Value	0	0	0		0	0	0	0

Bit No.	Bit Designator	Description
7	MMS	Master mode selection for configuring the source of synchronization trigger signal (TRGO) sent to the slave in master mode: 1: UE (update event) signal is used as TRGO. 0: OCxREF is used as TRGO.

6	ARPE	Auto-reload preload enable: 0: ARR register preload is not enabled. 1: ARR register preload is enabled.
5:4	CMS	Counter alignment mode selection: 00: Edge-aligned mode 01: Center-aligned mode 1; output compare interrupt flag is set only during counter down-counting down. 10: Center-aligned mode 2; output compare interrupt flag is set only during counter up-counting. 11: Center-aligned mode 3; output compare interrupt flag is set during both counter up-counting and down-counting.
3	CEN_ALL_EN	CEN_ALL enable: 1: The current GTIMER can be controlled by CEN_ALL. 0: The current GTIMER is not affected by the CEN_ALL signal.
2	DIR	Counting direction register: 0: Count up 1: Count down Note: This register is read-only when the timer is configured in center-aligned mode.
1	OPM	Single-pulse output mode: 0: The counter does not stop at the occurrence of an update event. 1: The counter stops at the occurrence of an update event (CEN is automatically cleared).
0	CEN	Counter enable: 0: Counter is disabled. 1: Counter is enabled.

13.3.2 GTIMER_CR1 Control Register

C901H/CA01H/CB01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CR1	PWMS_B_S		SOFT_BK	CEN_ALL	BKE_POL	BKE	PWM_DEAD	PWM_INV
R/W	R/W		R/W	W	R/W	R/W	R/W	R/W
Reset Value	0		0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:6	PWMS_B_S	Setting bit of PWM positive level status after PWM break trigger: 00: Low level

		01: High level 10/11: High-impedance state
5	SOFT_BK	Setting bit for software-triggered break function: 1: Software triggers the break function. 0: Software does not trigger the break function.
4	CEN_ALL	1: Enable GTIMER0/1/2 simultaneously. After writing this bit, the CEN bits of GTIMER0/1/2 will be set to 1 at the same time. 0: No operation. Reading this bit always returns 0.
3	BKE_POL	Break signal polarity configuration: 1: Break signal is active low. 0: Break signal is active high.
2	BKE	Break function enable: 1: Break function is enabled. 0: Break function is disabled.
1	PWM_DEAD	PWM dead-time insertion enable: 0: Dead-time avoidance function is disabled. 1: Dead-time avoidance function is enabled.
0	PWM_INV	Complementary PWM and original PWM differential enable: 0: Complementary PWM is in phase with the original PWM. 1: Complementary PWM is out of phase with the original PWM.

13.3.3 GTIMER_CR2 Control Register

C902H/CA02H/CB02H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CR2	-	BREAK2_SEL	BREAK1_SEL	PWMN_IDLE	PWMP_IDLE	MOE	PWMN_B_S	
R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	
Reset Value	0	0	0	0	0	0	0	

Bit No.	Bit Designator	Description
7	-	RSV: Not implemented, read as 0
6	BREAK2_SEL	**GTIMER0** IO pin break source selection: 1: Select the IO configured by GTIMER2 as the break source. 0: Do not select the IO configured by GTIMER2 as the break source.

		GTIMER1 IO pin break source selection: 1: Select the IO configured by GTIMER2 as the break source. 0: Do not select the IO configured by GTIMER2 as the break source. **GTIMER2** IO pin break source selection: 1: Select the IO configured by GTIMER1 as the break source. 0: Do not select the IO configured by GTIMER1 as the break source.
5	BREAK1_SEL	**GTIMER0** IO pin break source selection: 1: Select the IO configured by GTIMER1 as the break source. 0: Do not select the IO configured by GTIMER1 as the break source. **GTIMER1** IO pin break source selection: 1: Select the IO configured by GTIMER0 as the break source. 0: Do not select the IO configured by GTIMER0 as the break source. **GTIMER2** IO pin break source selection: 1: Select the IO configured by GTIMER0 as the break source. 0: Do not select the IO configured by GTIMER0 as the break source.
4	PWMN_IDLE	PWM output negative level idle state: 1: Level is high. 0: Level is low.
3	PWMP_IDLE	PWM output positive level idle state: 1: Level is high. 0: Level is low.
2	MOE	Output enable: 1: Output is globally enabled. 0: Output is disabled.

1:0	PWMN_B_S	Setting bit of PWM complementary level status after PWM break trigger: 00: Low level 01: High level 10/11: High-impedance state

13.3.4 GTIMER_CR3 Control Register

C903H/CA03H/CB03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CR3	-					COMP2_BKEN	COMP1_BKEN	COMP0_BKEN
R/W	R					R/W	R/W	R/W
Reset Value	0					0	0	0

Bit No.	Bit Designator	Description
7:3	--	RSV: Not implemented, read as 0
2	COMP2_BKEN	Enable COMP2 as break source: 1: Enable COMP2 as the break source. 0: Disable COMP2 as the break source.
1	COMP1_BKEN	Enable COMP1 as break source: 1: Enable COMP1 as the break source. 0: Disable COMP1 as the break source.
0	COMP0_BKEN	Enable COMP0 as break source: 1: Enable COMP0 as the brake source. 0: Disable COMP0 as the brake source.

13.3.5 GTIMER_IER Interrupt Enable Register

C904H/CA04H/CB04H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_IER	-					BKE_IE	CC1IE	UIE
R/W	R					R/W	R/W	R/W
Reset Value	0					0	0	0

Bit No.	Bit Designator	Description
7:3	--	RSV: Not implemented, read as 0
2	BKE_IE	Break interrupt enable: 1: Enable break interrupt. 0: Disable break interrupt.

1	CCIE	Capture/compare channel interrupt enable: 0: Disable capture/compare interrupt. 1: Enable capture/compare interrupt.
0	UIE	Update event interrupt enable: 0: Disable update event interrupt. 1: Enable update event interrupt.

13.3.6 GTIMER_SR Status Register

C905H/CA05H/CB05H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_SR	-					BKE_F	CCIF	UIF
R/W	R					R/W	R/W	R/W
Reset Value	0					0	0	0

Bit No.	Bit Designator	Description
7:3	--	RSV: Not implemented, read as 0
2	BKE_F	Break interrupt flag: 1: In break state 0: Not in break state Write 1 to clear this bit.
1	CCIF	Capture/compare channel interrupt flag: If the capture/compare channel is configured as output: CCIF is set when the count value equals the compare value (CCR), and is cleared by software writing 1. If the capture/compare channel is configured as input: CCIF is set when a capture event occurs, and is cleared by software writing 1 or automatically cleared by software reading GTIMER_CCR.
0	UIF	Update event interrupt flag: set by hardware and cleared by software writing 1. When an update event occurs, UIF is set and the shadow register is updated.

13.3.7 GTIMER_EGR Event Generation Register

C906H/CA06H/CB06H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_EGR	-							UG
R/W	R							W

Reset Value	0	0

Bit No.	Bit Designator	Description
7:1	--	RSV: Not implemented, read as 0
0	UG	Software update event: This bit can be set by software to generate an update event, and is automatically cleared by hardware. When the UG bit is set by software, the counter is reinitialized, the shadow register is updated, and the prescaler counter is cleared.

13.3.8 GTIMER_CCMR0 Capture/Compare Mode Register

C907H/CA07H/CB07H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCMR0	TFLT	TEDGE	TSSEL		-			CCS
R/W	R/W	R/W	R/W		R/W			R/W
Reset Value	0	0	0		0			0

Bit No.	Bit Designator	Description
7	TFLT	External count source filter enable: 0: No filtering function 1: Filtering function enabled
6	TEDGE	Count source edge selection: 0: Count on rising edge 1: Count on falling edge
5:4	TSSEL	Count source selection bits: **GTIMER0:** 00: PCLK 01: GTIMER2_TRG0 (synchronization trigger signal of GTIMER2) 10: CLK38K_GTIMER0 (38 kHz clock) 11: GTIMER0_CH (GTIMER0 capture input) **GTIMER1:** 00: PCLK 01: GTIMER0_TRG0 (synchronization trigger signal of GTIMER0) 10: CLK38K_GTIMER1 (38 kHz clock) 11: GTIMER1_CH (GTIMER1 capture input)

		GTIMER2: 00: PCLK 01: GTIMER2_TRG0 (synchronization trigger signal of GTIMER1) 10: CLK38K_GTIMER1 (38 kHz clock) 11: GTIMER2_CH (GTIMER2 capture input)
3:1	-	RSV: Not implemented, read as 0
0	CCS	Capture/compare channel 1 selection: 0: CC channel is configured as output. 1: CC channel is configured as input. Note: CCS can only be written when the channel is disabled (CCE = 0).

13.3.9 GTIMER_CCMR1 Capture/Compare Mode Register

C908H/CA08H/CB08H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCMR1	CAPCLR	ICPSC		CAPFLT	CAPEDGE		CAPSSEL	
R/W	R/W	R/W		R/W	R/W		R/W	
Reset Value	0	0		0	0		0	

Bit No.	Bit Designator	Description
7	CAPCLR	First-capture clear control bit: 0: The counter starts counting immediately after being enabled. 1: The counter remains at 0 after being enabled and does not start counting until the first edge is captured.
6:5	ICPSC	Capture source prescaler bits: 00: Divided by 1 01: Divided by 2 10: Divided by 4 11: Divided by 8
4	CAPFLT	Input capture signal filter enable: 0: No input filtering 1: Input filtering enabled
3:2	CAPEDGE	Capture edge trigger control bits: 00: Trigger on rising edge 01: Trigger on falling edge 10/11: Trigger on rising or falling edge

1:0	CAPSSEL	Capture source selection bits: **GTIMER0:** 00: GTIMER0_CH 01: UART0_RX 10: CLK38K_GTIMER0 11: LPTIMER_LPOUT0 **GTIMER1:** 00: GTIMER1_CH 01: UART1_RX 10: CLK38K_GTIMER1 11: LPTIMER_LPOUT1 **GTIMER2:** 00: GTIMER2_CH 01: UART2_RX 10: CLK38K_GTIMER2 11: UART3_RX

13.3.10 GTIMER_CCER Capture/Compare Enable Register

C909H/CA09H/CB09H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCER	-						CCP	CCE
R/W	R						R/W	R/W
Reset Value	0						0	0

Bit No.	Bit Designator	Description
7:3	--	RSV: Not implemented, read as 0.
1	CCP	CC Channel Polarity (when configured as output): 0: Output high level when CNT < CCR (CC channel output is in phase with OCxREF) 1: Output high level when CNT > CCR (CC channel output is out of phase with OCxREF)
0	CCE	Capture/compare output enable: **When CC channel is configured as output:** 0: OC output disabled 1: OC output enabled

		When CC channel is configured as input: 0: Capture function disabled 1: Capture function enabled

13.3.11 GTIMER_CNT0 Counter Register

C90AH/CA0AH/CB0AH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CNT0	CNT[7:0]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	CNT	Count value CNT [7:0]

13.3.12 GTIMER_CNT1 Counter Register

C90BH/CA0BH/CB0BH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CNT1	CNT[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	CNT	Count value CNT [15:8]

13.3.13 GTIMER_PSC0 Prescaler Register

C90CH/CA0CH/CB0CH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_PSC0	PSC[7:0]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	PSC	Counter clock (CK_CNT) prescaler value: $f_{CK\_CNT} = f_{CK\_PSC}/(PSC[15:0]+1)$

Note: Even if preload is not enabled, the PSC value will still not be loaded into the shadow register until an update event occurs.

13.3.14 GTIMER_PSC1 Prescaler Register

C90DH/CA0DH/CB0DH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_PSC1	PSC[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	PSC	Counter clock (CK_CNT) prescaler value: $f_{CK\_CNT} = f_{CK\_PSC}/(PSC[15:0]+1)$

Note: Even if preload is not enabled, the PSC value will still not be loaded into the shadow register until an update event occurs.

13.3.15 GTIMER_ARR0 Auto-reload Register

C90EH/CA0EH/CB0EH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_ARR0	ARR[7:0]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	ARR	Auto-reload value on counter overflow This is a preload register whose content is loaded into the shadow register upon an update event.

13.3.16 GTIMER_ARR1 Auto-reload Register

C90FH/CA0FH/CB0FH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_ARR1	ARR[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	ARR	Auto-reload value on counter overflow This is a preload register whose content is loaded into the shadow register upon an update event.

13.3.17 GTIMER_ARR2 Auto-reload Register

C910H/CA10H/CB10H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_ARR2	ARRN[7:0]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	ARRN	Auto-reload value on counter overflow, complementary counter This is a preload register whose content is loaded into the shadow register at each update event.

13.3.18 GTIMER_ARR3 Auto-reload Register

C911H/CA11H/CB11H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_ARR3	ARRN[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	ARRN	Auto-reload value on counter overflow, complementary counter This is a preload register whose content is loaded into the shadow register upon an update event.

13.3.19 GTIMER_CCR0 Capture/Compare Register

C912H/CA12H/CB12H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCR0	CCR[7:0]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	CCR	Capture/compare channel register **If the channel is configured as output:** This is a preload register whose content is loaded into the shadow register and then used to compare with the counter to generate OC output.

		If the channel is configured as input: CCR stores the counter value measured at the latest input capture event, and the CCR is read-only in this case.

13.3.20 GTIMER_CCR1 Capture/Compare Register

C913H/CA13H/CB13H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCR1	CCR[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	CCR	Capture/compare channel register **If the channel is configured as output:** This is a preload register whose content is loaded into the shadow register and then used to compare with the counter to generate OC output. **If the channel is configured as input:** CCR stores the counter value measured at the latest input capture event, and the CCR is read-only in this case.

13.3.21 GTIMER_CCR2 Capture/Compare Register

C914H/CA14H/CB14H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCR2	CCRN[7:0]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	CCRM	Capture/compare channel register, complementary counter **If the channel is configured as output:** This is a preload register whose content is loaded into the shadow register and then used to compare with the counter to generate OC output.

13.3.22 GTIMER_CCR3 Capture/Compare Register

C915H/CA15H/CB15H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
GTIMER_CCR3	CCRN[15:8]							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	CCRM	Capture/compare channel register, complementary counter **If the channel is configured as output:** This is a preload register whose content is loaded into the shadow register and then used to compare with the counter to generate OC output.

13.4 Usage Instructions

13.4.1 Counter Operating Mode

Counting direction:

1. Up-counting mode

   In up-counting mode, the counter counts from 0 to the auto-reload value, then restarts from 0 and generates an interrupt. At this time, an update event (UEV) is generated. The load register inside the chip can be updated only when the UEV occurs.

2. Down-counting mode

   In down-counting mode, the counter counts from the auto-reload value down to 0, then restarts from the auto-reload value and generates an interrupt. At this time, the update event (UEV) is generated. The load register inside the chip can be updated only when the UEV occurs.

3. Center-aligned mode (up/down counting)

   - In center-aligned mode, the counter counts from 0 to (auto-reload value - 1), generates an interrupt; next counts from the auto-reload value down to 1 and generates another interrupt; then it restarts counting from 0.
   - In this mode, the DIR direction bit in the register cannot be written.
   - The UEV can be generated at each counter overflow and underflow. The load register inside the chip can be updated only when the UEV occurs.

13.4.2 Input Capture Mode

In input capture mode, the capture register (CCR) stores the current counter value when a trigger edge appears on the corresponding ICx signal. After a capture occurs, the corresponding interrupt flag is set, and a capture interrupt is generated simultaneously. CCxIF is cleared by software. The trigger edge can be controlled by the register as a rising edge or a falling edge. The capture source can be filtered or unfiltered.

13.4.3 PWM Mode

PWM mode can generate waveforms with the frequency determined by the values of ARR and PSC, as well as the duty cycle determined by the value of CCR.

In up-counting mode, OCxREF is set high when CNT < CCR, otherwise low; in down-counting mode, OCxREF is set low when CNT > CCR, otherwise high.

- PWM edge-aligned mode

  In up-counting mode, when the timer is configured in PWM mode 1 with CCP = 0, OCxREF is high while CNT < CCR and low otherwise. If CCR ≥ ARR, OCxREF remains high; if CCR = 0, OCxREF remains low. And OCxREF will be held at 1 if CCR > ARR and held at 0 if CCR = 0.

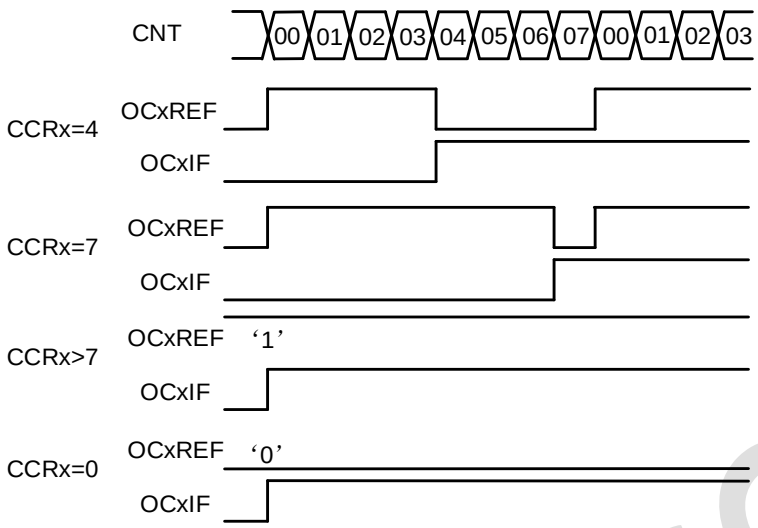


Figure 13-2: Edge-aligned PWM Waveform (ARR = 7)

- PWM center-aligned mode

  The definition of OCxREF level is identical to that in edge-aligned mode. An example waveform is shown below:

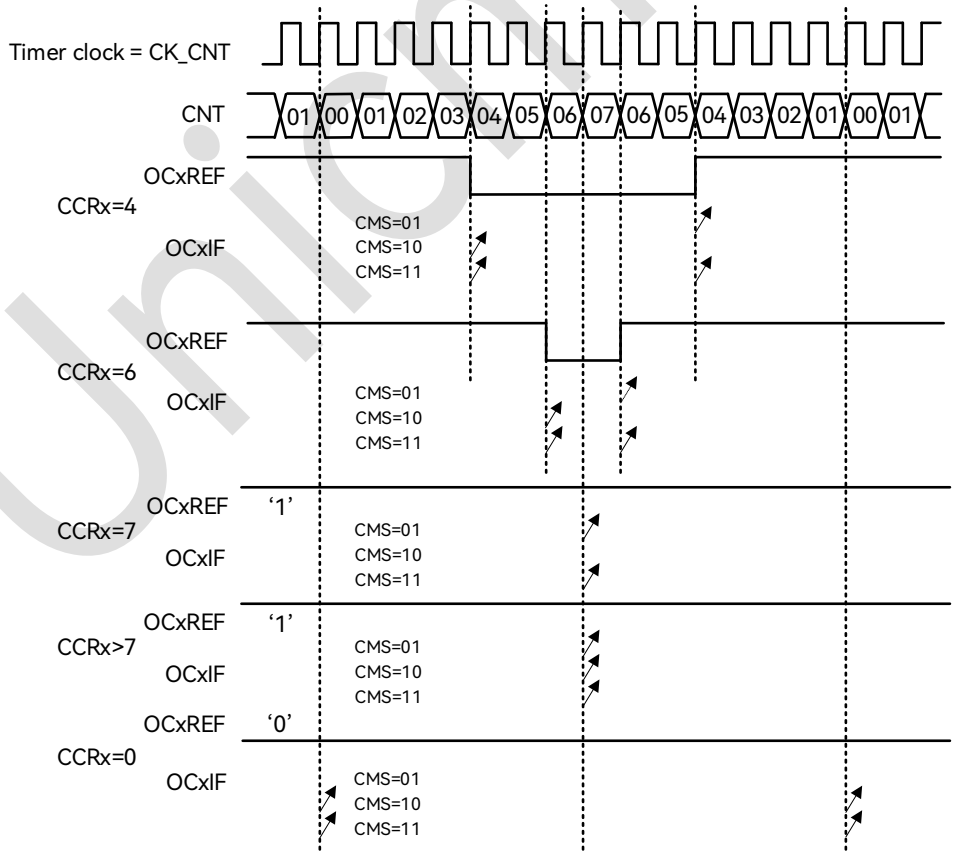


Figure 13-3: Center-aligned PWM Waveform (ARR = 7)

As the function of complementary PWM with dead-time insertion is enabled, the frequency of the PWM output signal depends on the ARR register and the PSC register. The maximum value of the count is determined by the larger of the ARR and ARRN values stored in the ARR register. The duty cycle is determined by the CCR register.

The OCxREF output signal is as follows:

1. In edge-aligned down-counting mode (DIR = 1), OCxREF outputs high level when (MAX (ARR, ARRN) - ARR) ≤ CNT ≤ CCR; otherwise, it outputs low level.
2. In edge-aligned up-counting mode (DIR = 0), OCxREF outputs high level when CNT < CCR or CNT > ARR or software writes UG; otherwise, it outputs low level.
3. In center-aligned mode, OCxREF outputs high level when CNT≤ CCR in down-counting (DIR = 1) or when CNT < CCR in up-counting (DIR = 0); otherwise, it outputs low level.
4. When MIN(CCR, CCRN) = MAX(ARR, ARRN), OCxREF outputs low level when CNT = ARR in edge-aligned up-counting mode; otherwise, it outputs high level.
5. When MIN(CCR, CCRN) > MAX(ARR, ARRN), OCxREF always outputs high level.
6. When MIN(CCR, CCRN) = 0, in edge-aligned down-counting mode, the output behavior of OCxREF is the same as that specified in item 1; otherwise, it outputs low level.

The OCxREFn output signal is as follows:

1. In edge-aligned down-counting mode (DIR = 1), OCxREFn outputs high level when (MAX (ARRN, ARRN) - ARR) ≤ CNT ≤ CCRN; otherwise, it outputs low level.
2. In edge-aligned up-counting mode (DIR = 0), OCxREFn outputs high level when CNT < CCRN or CNT > ARRN or software writes UG; otherwise, it outputs low level.
3. In center-aligned mode, OCxREFn outputs high level when CNT≤ CCRN in down-counting (DIR = 1) or when CNT < CCRN in up-counting (DIR = 0); otherwise, it outputs low level.

4. When MIN(CCR, CCRN) = MAX(ARRN, ARRN), OCxREFn outputs low level when CNT = ARR in edge-aligned up-counting mode; otherwise, it outputs high level.
5. When MIN(CCR, CCRN) > MAX(ARR, ARRN), OCxREFn always outputs high level.
6. When MIN(CCR, CCRN) = 0, in edge-aligned down-counting mode, the output behavior of OCxREFn is the same as that specified in item 1; otherwise, it outputs low level.

13.4.4 Break Function

The PWM waveform output can be triggered to stop (break) by software writing to the SOFT_BK bit or by hardware trigger via external IO. After the PWM output is stopped by a break signal, it is required to clear the BKE_F bit first and then enable the MOE bit to resume the PWM output.

13.5 Operating Procedures

13.5.1 General-purpose Timer

1. Configure PCLK1 and PRESET1 to enable GTIMER and release the reset.
2. Configure GTIMER_PSC to set the prescaler value.
3. Configure GTIMER_ARR to set the auto-reload value.
4. Configure GTIMER_EGR to generate an update event to immediately load the PSC value into the shadow register.
5. Clear the interrupt flag generated by the update event.
6. Configure GTIMER_CRO to enable GTIMER counting.

13.5.2 PWM Output

1. Multiplex IO into GTIMER_CH and GTIMER_CHN according to the IO multiplexing relation.
2. Configure PCLK1 and PRESET1 to enable GTIMER and release the reset.
3. Configure GTIMER_PSC to set the prescaler value.
4. Configure GTIMER_ARR to set the auto-reload value.
5. Configure GTIMER_CCR to set the compare value.
6. If complementary PWM output is required, configure GTIMER_ARRN and GTIMER_CCRN.
7. Configure GTIMER_EGR to generate an update event to immediately load the PSC value into the shadow register.
8. Clear the interrupt flag generated by the update event.
9. Configure GTIMER_CCER to enable OC output.
10. Configure GTIMER_CR2 to enable the main output.
11. Configure GTIMER_CRO to enable GTIMER counting.

13.5.3 Input Capture

1. Multiplex IO into GTIMER_CH according to the IO multiplexing relation.
2. Configure PCLK1 and PRESET1 to enable GTIMER and release the reset.
3. Configure GTIMER_PSC to set the prescaler value.
4. Configure GTIMER_ARR to set the auto-reload value.
5. Configure GTIMER_CCMR1 to set the CC channel as input, select the capture source, set the capture source prescaler, and configure the capture edge trigger control.

6. If capture interrupt is required, configure GTIMER0_IER to enable the capture/compare interrupt.
7. Configure GTIMER_CCER to enable the capture function.
8. Configure GTIMER_CRO to enable GTIMER counting.

13.5.4 Break Function

1. Multiplex IO into GTIMER_BKE according to the IO multiplexing relation.
2. Configure PCLK1 and PRESET1 to enable GTIMER and release the reset.
3. Configure GTIMER_CR1 to set the positive level status of PWM after a PWM break trigger.
4. Configure GTIMER0_CR1 to select the break signal polarity.
5. Configure GTIMER_IER to enable the break interrupt if it is required.
6. Configure GTIMER0_CR1 to enable the break function.
7. Configure GTIMER_CRO to enable GTIMER counting.

14 I2C

14.1 Overview

The I2C bus interface connects the microcontroller to the serial I2C bus. The I2C module receives and transmits data, converting it from serial to parallel or vice versa. It is connected to the I2C bus via the data pin SDA and the clock pin SCL to control all I2C bus-specific timing sequences. This module supports both master mode and slave mode.

14.2 Main Features

- I2C as master
- I2C as slave
- Programmable I2C slave address
- Detection of SDA transitions when SCL is low
- Programmable NACK/ACK response
- Input SCL bus filter function
- Standard/Fast/HS modes available
- 7-bit device addressing
- Multi-master mode

14.3 Register Description

I2C register base address: 0xCC00

Table 14-1: List of Registers

Offset	Name	Description
0x00	I2C_SLAVE_ADDR1	I2C slave address register 1
0x01	I2C_CLK_DIV	I2C SCL clock divider register
0x02	I2C_CR0	Control register 0
0x03	I2C_CR1	Control register 1
0x04	I2C_SR0	Status register 0
0x05	I2C_SR1	Status register 1
0x06	I2C_DR	Data register
0x07	I2C_SLAVE_ADDR2	I2C slave address register 2

14.3.1 I2C_SLAVE_ADDR1 Slave Address Register 1

CC00H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_SLAVE_ADDR1	ADD1[7:1]							RSV
R/W	R/W							R
Reset Value	0							0

Bit No.	Bit Designator	Description
7:1	ADD1[7:1]	Bits 7–1 of the address
0	RSV	Reserved

14.3.2 I2C_CLK_DIV Clock Divider Register

CC01H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_CLK_DIV	I2C_CLK_DIV							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	2C_CLK_DIV	SCL prescaler value: The I2C transmission rate is set by configuring this register.

		$f_{scl} = (f_{sysclk}) / (4 * (DIV\ register\ value + 1))$

14.3.3 I2C_CR0 Control Register 0

CC02H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_CR0	MAAS1_INT_En	MIEN	RSTA	TACK	MTX	MSTA	RSV	MEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	MAAS1_INT_En	MAAS1 (received device address matches slave address register 1) interrupt enable: 0: MAAS1 interrupt disabled 1: MAAS1 interrupt enabled
6	MIEN	MTF (byte data (including address) being transferred) interrupt enable: 0: MTF interrupt disabled 1: MTF interrupt enabled
5	RSTA	RSTA generation bit: 0: No condition for repeating start is generated. 1: After writing 1, a start condition is generated upon completion of transmitting or receiving a byte.
4	TACK	Transmit acknowledge bit / Stop condition bit: **In master mode:** 0: An ACK is generated during the acknowledge cycle after receiving a byte. 1: The master will generate a STOP condition after transmitting the current byte. **In slave mode:** 0: An ACK is generated during the acknowledge cycle after receiving a byte. 1: An NACK is generated during the acknowledge cycle after receiving a byte.
3	MTX	0: The device operates as receiver. 1: The device operates as transmitter.

		When acting as a slave, the processor shall query the SRW bit in I2C_SR to determine whether to function as a transmitter or receiver, and then set the MTX bit accordingly.
2	MSTA	Master/slave selection bit, START bit: 0: Slave mode 1: Master mode If this bit changes from 0 to 1, the module generates a START condition. MSTA is cleared when a STOP condition is generated or when a slave address match occurs (MAAS1 or MAAS2 = 1).
1	HOLD_EN	1: Enable this bit, after receiving an address match interrupt, wait for the MTF signal to be 1 before writing data.
0	MEN	0: Device disabled 1: Device enabled

14.3.4 I2C_CR1 Control Register 1

CC03H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_CR1	RSV	MTX_ANTO_EN	OD_MODE	RSV	MAAS2_INT_EN	WBT_INT_EN	RXNE_INT_EN	TXE_INT_EN
R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	RSV	Reserved
6	MTX_ANTO_EN	● When the module operates in slave mode, the SDA line for transmitting data and address switches automatically. ● When the module operates in slave mode, setting this bit to 1 allows the SDA transfer direction to switch automatically according to the RW bit on the bus after the master device completes address transmission. 0: Auto-switch function disabled 1: Auto-switch function enabled
5	OD_MODE	SCL and SDA output mode selection: 0: Push-pull mode output 1: Open-drain mode output
4	RSV	Reserved

3	MAAS2_INT_EN	MAAS2 (received device address matches slave address register 2) interrupt enable: 0: MAAS2 interrupt disabled 1: MAAS2 interrupt enabled
2	WBT_INT_EN	WBT (byte has been transferred and TXE or RXNE is 1) interrupt enable: 0: WBT interrupt disabled 1: WBT interrupt enabled
1	RXNE_INT_EN	RXNE (receive data register not empty) interrupt enable: 0: RXNE interrupt disabled 1: RXNE interrupt enabled
0	TXE_INT_EN	TXE (transmit data register not empty) interrupt enable: 0: TXE interrupt disabled 1: TXE interrupt enabled

14.3.5 I2C_SR0 Status Register 0

CC04H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_SR0	MAAS2	MTF	MAAS1	MBB	RSV	SRW	MTF_H	RACK
R/W	R/W	R/W	R/W	R	R	R	R/W	R
Reset Value	0	0	0	0	0	0	0	1

Bit No.	Bit Designator	Description
7	MAAS2	0: Device address 2 does not match the received address. 1: Device address 2 matches the received address. Write 1 to clear this bit.
6	MTF	0: Byte transfer is not completed. 1: Byte transfer is completed. This bit is 0 when a byte of data (including address) is being transmitted, and is set to 1 at the falling edge of the 9th SCL clock (ACK cycle) after a byte transmission is completed. Writing 1 clears it half an SCL cycle later than MTF_H.
5	MAAS1	0: Device address 1 does not match the received address. 1: Device address 1 matches the received address. Write 1 to clear this bit.
4	MBB	0: No data communication on the bus (this bit is cleared when a STOP flag is detected on the bus)

		1: Data communication being in progress on the bus (this bit is set to 1 when a START flag is detected on the bus)
3	RSV	Reserved
2	SRW	0: Not serving as slave transmitter 1: Serving as slave transmitter ● After the address matches, SRW indicates the R/W bit in the address call command, which is only valid under the following conditions: a complete transfer has finished, no new transfer has been started, and the I2C is configured as a slave with the slave address matched. ● This bit is automatically cleared when a STOP condition or a repeated START condition is detected.
1	MTF_H	Fast byte transfer complete flag: 0: Fast byte transfer not yet completed (half an SCL cycle earlier) 1: Fast byte transfer completed MTF_H is generated at the rising edge of the 9th SCL clock (ACK cycle), half an SCL cycle earlier than MTF. This bit can be cleared by writing 1 or writing MTF to 1.
0	RACK	Acknowledge receive status bit: 0: ACK received in the most recent transmit acknowledge cycle 1: NACK received in the most recent transmit acknowledge cycle The RACK bit can be cleared only by a START condition.

14.3.6 I2C_SR1 Status Register 1

CC05H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_SR1	RSV					WBT	RXNE	TXE
R/W	R					R/W	R/W	R/W
Reset Value	0					0	0	0

Bit No.	Bit Designator	Description
7:3	RSV	Reserved
2	WBT	0: Byte transfer not yet completed, or completed but neither TXE nor RXNE is set. 1: Byte transfer completed and either TXE or RXNE is set. This bit can be cleared by reading/writing the data register I2C_DR, or by writing 1.

1	RXNE	0: Receive data register empty 1: Receive data register not empty This bit can be set by hardware, and can be cleared by reading the data register I2C_DR or by writing 1.
0	TXE	0: Transmit data register not empty 1: Transmit data register empty This bit can be set by hardware, and can be cleared by writing the data register I2C_DR or by writing 1.

14.3.7 I2C_DR Data Register

CC06H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_DR	I2CDR							
R/W	R/W							
Reset Value	0							

Bit No.	Bit Designator	Description
7:0	I2CDR	I2C data register value

14.3.8 I2C_SLAVE_ADDR2 Slave Address Register 2

CC07H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
I2C_SLAVE_ADDR2	ADD2[7:1]							ADDR2_EN
R/W	R/W							R/W
Reset Value	0							0

Bit No.	Bit Designator	Description
7:1	ADD2[7:1]	Bits 7−1 of the address
0	ADDR2_EN	0: SLAVE_ADDR2 address matching disabled 1: SLAVE_ADDR2 address matching enabled

14.4 Functional Description

14.4.1 Mode Selection

The module defaults to slave mode and switches to master mode when a START operation is initiated by software. In master mode, I2C starts data transfer, generates the clock signal, and can send a STOP signal to terminate the transfer. In slave mode, I2C can recognize its own 7-bit address. Data and addresses are transmitted in 8-bit byte, with the most significant bit (MSB) first.

The start condition is followed by address, which is only transmitted in the master mode. The receiver must return an ACK to the transmitter during the 9th clock cycle after 8 clock cycles of a byte transfer. See the diagram below:

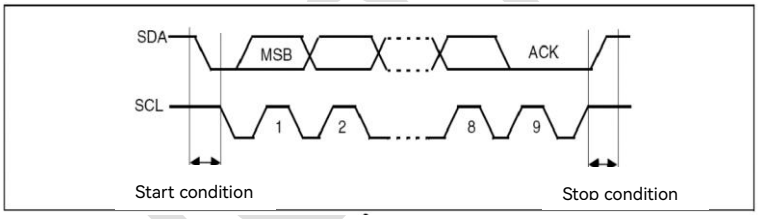


Figure 14-1: Slave Mode Timing Diagram

14.4.2 I2C Slave Mode

Once the start condition is detected, the address received on the SDA line is sent to the shift register, and then compared with the own device address of the chip. If the address does not match, I2C ignores it and waits for another start condition. If the address matches, the controller checks the transfer direction via the SRW bit and proceeds as follows:

- **Slave transmitter**

  The transmitter loads the byte from the data register to the internal shift register and sends it to the SDA line, generating the transmit data register empty flag (TXE), which can be

cleared by software updating the data register.

After receiving an ACK pulse, if no new data is written to the data register before the next data transmission ends, i.e., TXE remains 1, the byte-wait flag bit (WBT) is set to 1, and the I2C interface holds SCL low until new data is written to the data register.

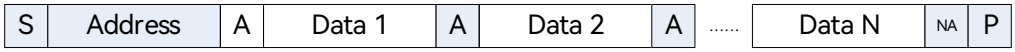


Figure 14-2: Transmission Diagram of 7-bit Slave Transmitter

Note: S = Start (start condition), P = Stop (stop condition), A = Acknowledge, NA = No acknowledge.

: From master to slave

: From slave to master

- **Slave receiver**

After receiving data, the slave receiver latches the byte received from the SDA line via the internal shift register into the data register, generating the data register not empty flag (RXNE), which can be cleared by software reading the value of the data register.

The I2C interface generates an ACK pulse after receiving each byte.

If the value in the data register is not read before receiving new data (i.e., RXNE remains 1), the byte-wait flag bit (WBT) is set to 1, and the I2C interface holds SCL low until the value in the data register is read.

Figure 14-3: Transmission Diagram of 7-bit Slave Receiver

Note: S = Start (start condition), P = Stop (stop condition), A = Acknowledge, NA = No acknowledge.

- **Terminating slave communication**

  After the last byte is transferred, the master issues a stop operation, and the I2C interface releases the SCL and SDA lines upon detecting the stop condition.

14.4.3 I2C Master Mode

In master mode, the I2C interface initiates data transfer and generates the clock signal. The serial data transfer always starts with a start condition and ends with a stop condition. When a start operation is initiated on the bus via the START bit, the device enters the master mode.

Operations in the master mode are as follows:

1. Configure the clock control register.
2. Configure the data register (which internally stores the slave address and the R/W bit).
3. Set the MSTA bit of the control register to 1 to generate a start condition.

- **Master transmitter:**

  After transmitting the address, the master loads the byte from the data register to the SDA line via the internal shift register, generating the transmit data register empty flag (TXE), which can be cleared by software updating the data register.

  Upon receiving an acknowledge pulse, it confirms that new data has been transmitted to the data register. If new data has not been written to the data register before the next data transmission ends (i.e., TXE remains 1), the byte wait flag (WBT) is set to 1, and the I2C interface holds SCL low until new data is written to the data register.

  The master then issues a STOP signal to generate a stop condition.

Figure 14-4: Transmission Diagram of 7-bit Master Transmitter

Note: S = Start (start condition), P = Stop (stop condition), A = Acknowledge, NA = No acknowledge.

- **Master receiver:**

  After transmitting the address, the I2C interface latches the data byte received from the SDA line to the data register via the internal shift register, generating the data register not empty flag (RXNE), which can be cleared by software reading the value of the data register.

  If the value in the data register is not read before receiving new data (i.e., RXNE remains 1), the byte-wait flag bit (WBT) is set to 1, and the I2C interface holds SCL low until the value in the data register is read.

  After receiving each byte, the master sends an ACK pulse and confirms that the value in the data register has been read.

  The master sends a NACK after the slave receives the last byte. Upon receiving the NACK, the slave releases the control of the SCL and SDA lines. Then the master can send a stop/repeated start condition.

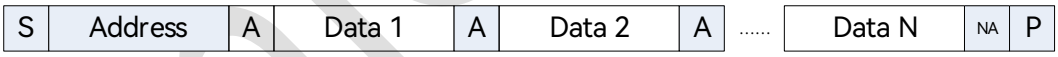


Figure 14-5: Transmission Diagram of 7-bit Master Receiver

Clock stretching:

- Transmit mode: SCL is held low while the data register is empty (TXE = 1) waiting for new data.
- Receive mode: SCL is held low while the data register is full (RXNE = 1) waiting for the CPU to read the old data.

14.4.4 SCL Bus Filter Algorithm 0

When SCL_FILTER_SEL is 0 and the value of I2C_FILTER register is 0, SCL is not provided with the filter function. When the value is not 0, the filtering time = t_{cntc} * I2C_FILTER. Wherein, t_{cntc} is the clock period of PCLK divided by 8.

Example:

When I2C_FILTER = 2, the SCL signal must be sampled as a high level for two consecutive t_{cntc} durations to be output as high level, as pulses with a width of less than two t_{cntc} are considered as interference glitches and filtered out.

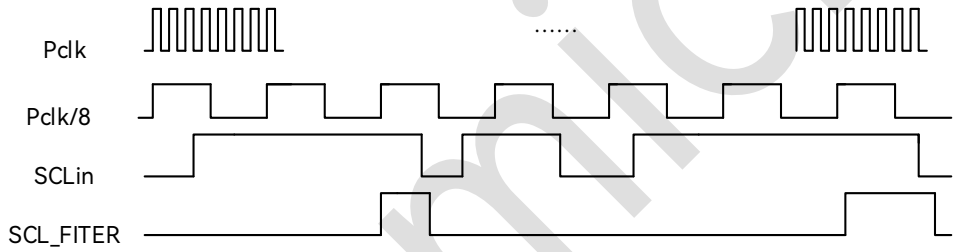


Figure 14-6: Example of SCL Bus Filter Algorithm 0

Note:

- During operation, set SDA_IN_DELAY to the same value as SCL_FILTER. After filtering, the SDA and SCL signals will maintain the same phase as in the input.
- During communication, the SCL filtering only filters high-level signals with a duration shorter than t_{cntc} * I2C_FILTER, and does not filter low-level signals. When not in communication, the SCL filtering only filters low-level signals with a duration shorter than t_{cntc} * I2C_FILTER, and does not filter high-level signals. The level targeted by the SCL filtering function switches automatically according to the START bit.

14.4.5 SCL Bus Filter Algorithm 1

If SCL_FILTER_SEL = 1, SCL filter algorithm 1 is enabled. The maximum width of glitches to be filtered is t_{fclk} x SWIDTH_THOLD. FREEZE_THOLD is the upper limit of the filter count, and when adopting SCL filter algorithm 1, ensure SWIDTH_THOLD < FREEZE_THOLD. Similar to algorithm 0, SDA_IN_DELAY can be adopted to delay the SDA signal.

14.4.6 Detecting SDA Transitions When SCL is Low

If I2C_DET = 0, the detection function is disabled. If I2C_DET ≠ 0, the detection function is enabled. When SCL is slow and the number of detected SDA rising-edge transitions exceeds the value in the I2C_DET register, set the DETR bit in I2C_SR to 1.

Example:

When I2C_DET = 5, the internal counter starts counting when SCL is low. If the number of SDA rising-edge transitions reaches 5 or more, DETR = 1. When SCL goes high, the internal counter is cleared and waits for the next low level of SCL to restart counting. As illustrated in the diagram below:

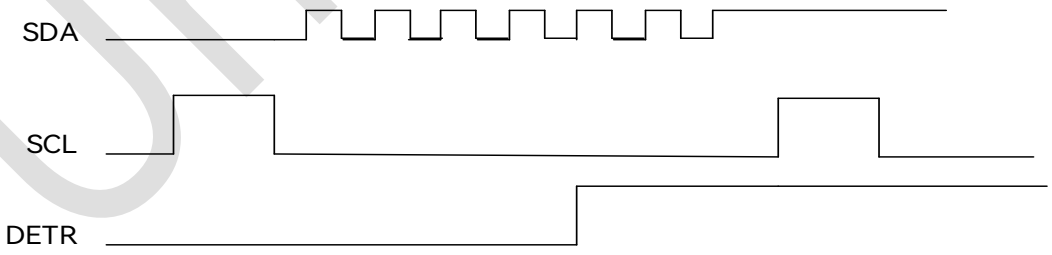


Figure 14-7: SDA Transition Timing Diagram

14.5 Operating Procedure

14.5.1 Initialization

1. Configure PCLK0 and PRESET0 to enable I2C and release the reset.
2. Multiplex IO into I2C_SDA and I2C_SCL according to the IO multiplexing relation, and configure PxPUN to enable the internal pull-up resistor.
3. Configure I2C_CR1 to enable the open-drain mode.
4. Configure the value of I2C_CLK_DIV register to determine the I2C transfer rate.
5. In the case of serving as slave, configure REG_I2C_CR1 to enable automatic switching of SDA transfer direction in slave mode, and configure REG_I2C_CR0 to enable hold_en.
6. Configure I2C_CR0 to enable I2C.

14.5.2 Master Transmitter

1. Write the 7-bit slave address to be accessed by I2C to the I2C_DR register.
2. Set MTX, MEN and MSTA bits to 1 in the I2C_CR0 register to initiate a START condition.
3. When TXE is read as 1, the first byte to be transmitted can be written to the I2C_DR register, and the hardware will clear the TXE bit simultaneously.
4. Wait for the MTF flag and check if an ACK is received to confirm the slave is responsive. If a NACK is received, the hardware will automatically issue a STOP condition and release the bus, and the software shall wait for MBB to be 0 before exiting.
5. Repeat steps 3 and 4.
6. After writing the last byte to I2C_DR, wait until the penultimate byte is transmitted (MTF ==

1), then set TACK = 1 in the I2C_CR register to indicate that the transmission is about to end. If a restart operation is required, set RSTA to 1 at this point.

7. After the last byte is transmitted, if RSTA = 1, a Restart flag is issued and data transmission continues; if RSTA = 0, the hardware automatically generates a STOP condition, and the software waits for MBB to be 0 before exiting.

Note: The above is the standard transmission flow for the master transmitter (no clock stretching occurs). If there is clock stretching (WBT == 1), the software must handle it immediately, otherwise the SCL clock will stop.

14.5.3 Master Receiver

1. Write the 7-bit slave address to be accessed by I2C plus a 1-bit value of 1 into the I2C_DR register, indicating that the master acts as a receiver.
2. Set MTX, MEN and MSTA bits to 1 in the I2C_CR register to initiate a START condition.
3. Wait for the MTF flag and check if an ACK is received to confirm the slave is responsive. If a NACK is received, the master will automatically issue a STOP condition and release the bus, and the software shall wait for MBB to be 0 before exiting.
4. When RXNE is read as 1, the processor shall read the bytes received from the I2C_DR register, and the hardware will clear the RXNE bit simultaneously. Wait until the next byte is completely received.
5. Wait for the MTF flag and clear it via software (the software flow can continue even without clearing it).
6. Repeat steps 4 and 5.
7. When the penultimate byte is received and the ACK signal (i.e., the penultimate MTF flag) is transmitted, the master sets TACK = 1 in the I2C_CR register to indicate that the next byte

to be received is the last one.

8. After the last byte is received, the hardware automatically issues a NACK signal and generates a STOP condition, and the software waits for MBB to be 0 before exiting.

Note: The above is the standard transmission flow for the master receiver (no clock stretching occurs). If there is clock stretching (WBT == 1), the software must handle it immediately, otherwise the SCL clock will stop.

14.5.4 Slave Transmitter

1. Write a 7-bit address into the I2C_SLAVE_ADDR1 or I2C_SLAVE_ADDR2 register as the address to be addressed in the slave mode.
2. Set MEN = 1 in the I2C_CR register to enable the I2C module.
3. Wait for the MAAS1 or MASS2 (ADDR2_EN = 1) flag to be valid. Repeat step 3 if the address match is invalid.
4. If the address match is valid, check the SRW bit: 0: act as slave receiver; 1: act as slave transmitter.
5. Wait for the byte transmission complete flag (MTF).
6. Write the first data byte to be transmitted into I2C_DR, and set MTX = 1 in the I2C_CR register to indicate that the slave acts as a transmitter.
7. When TXE is read as 1, the second byte to be transmitted can be written to the I2C_DR register, and the hardware will clear the TXE bit simultaneously.
8. Wait for the MTF flag and check if an ACK is received to confirm the master is responsive.
9. Repeat steps 7 and 8. After receiving the NACK or STOP signal from the master, the I2C module releases the bus. The software waits for MBB to be 0 and then exits.

14.5.5 Slave Receiver

1. Write a 7-bit address to the I2C_SLAVE_ADDR1 or I2C_SLAVE_ADDR2 register as the address to be addressed in the slave mode.
2. Set MEN = 1 in the I2C_CR register to enable the I2C module.
3. Wait for the MAAS1 or MASS2 (ADDR2_EN = 1) flag to be valid. Repeat step 3 if the address match is invalid.
4. If the address match is valid, check the SRW bit: 0: act as slave receiver; 1: act as slave transmitter.
5. Wait for the byte transmission complete flag (MTF).
6. When RXNE is read as 1, the processor shall read the bytes received from the I2C_DR register, and the hardware will clear the RXNE bit simultaneously. Wait until the next byte is completely received.
7. Wait for the MTF flag and clear it via software (the software flow can continue even without clearing it).
8. Repeat steps 6 and 7 until a STOP signal is received.
9. The I2C can also complete a byte reception and sending (i.e., MTF == 1). By setting TACK = 1 in the I2C_CR register, a NACK signal will be transmitted to the master upon reception of the next byte. The software waits for MBB to be 0 and then exits.

Note: The default I2C pins are P04 and P10, which shall first be configured to 0 before multiplexing other IO pins for I2C function.

15 Analog-to-Digital Converter (ADC)

15.1 Main Features

- 12-bit resolution
- Optional reference voltage: V_{DDA} or external V_{REF}
- Up to 8 analog channel inputs, with channels 0–6 as external inputs and channel 7 input source fixed as internal LDO
- Sampling rate: 1 Msps
- ADC supply/reference source configurable as V_{DDH} or external V_{REF} (when configured to 1, pin P2_5 serves as the external reference input)

15.2 Register Description

Table 15-1: List of Registers

Address	Name	Description
93H	ADC_IER	Interrupt enable register
ACH	ADC_GCR0	Control enable register
ADH	ADC_GCR1	Power-down enable register
B4H	ADC_GCR2	Configuration register
B5H	ADC_GCR3	Sampling register
B6H	ADC_DR0	Data low register
B7H	ADC_DR1	Data high register
F5H	ADC_HL	Channel setting register
F6H	ADC_CSTAT	Start register
F7H	ADC_SPW	Sampling clock pulse width configuration register
FDH	ADC_VREF	Voltage reference source selection register
FEH	ADC_CDR0	Clock division register 0
FFH	ADC_CDR1	Clock division register 1

15.2.1 ADC_IER Interrupt Enable Register

93H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_IER	-	-	-	-	-	-	-	RXINTEN
R/W	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:1	-	-
0	RXINTEN	RX BUF with valid data interrupt enable bit: 1: Interrupt enabled 0: Interrupt disabled

15.2.2 ADC_GCR0 Control Register

ACH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_GCR0	-	ADCCLKSEL	ADCRCEN	-	-	-	ADCCUNSET	ADCEN
R/W	R	R/W	R/W	R	R	R	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	-	-
6	ADCCLKSEL	ADC clock source selection: 0: Clock generated by internal clock divider 1: Clock generated by system clock generator (inverted phase)
5	ADCRCEN	ADC data register (ADCDRx) read-clear enable: 0: Disable clearing of ADC data register after reading. 1: Enable clearing of ADC data register after reading.
4:2	-	-
1	ADCCUNSET	Continuous mode setting: 1: ADC operates in continuous mode. 0: ADC operates in single-shot mode.
0	ADCEN	ADC controller enable: 0: Disable ADC module. 1: Enable ADC module.

15.2.3 ADC_GCR1 Power-down Enable Register

ADH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_GCR1	-	-	-	-	-	ADCSTEN	ADCRST	ADCPDEN
R/W	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1

Bit No.	Bit Designator	Description
7:3	-	-
2	ADCSTEN	ADC conversion start enable: A low-to-high transition starts the conversion. A high-to-low transition marks its end. In continuous mode, this bit is set automatically. It is cleared when ADC_EN = 0. Default value: 0
1	ADCRST	ADC internal digital-logic reset: 1: SAR ADC is held in reset. 0: SAR ADC is released from reset.
0	ADCPDEN	SAR SAR power-down enable: 0: SAR ADC is powered on. 1: SAR ADC is powered down.

15.2.4 ADC_GCR2 Configuration Register

B4H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_GCR2	-	-	ADC_PS	P1_2_SEL	CHEN			
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:4	-	-
5	ADC_PS	Analog ADC configuration parameters
4	P1_2_SEL	When this bit is 1, P1_2 is selected as the sampling channel for channel 0; when this bit is 0, P1_4 is selected as the sampling channel for channel 0.
3:0	CHEN	Enable relevant ADC channels for analog-to-digital conversion. Default value: 0 0001: Channel 0

		0010: Channel 1 0011: Channel 2 0100: Channel 3 0101: Channel 4 0110: Channel 5 0111: Channel 6 1000: Channel 7 0000: Reserved

15.2.5 ADC_GCR3 Sampling Register

B5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_GCR3	-	-	-	-	-	-	-	SAMPNEG
R/W	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:1	-	-
0	SAMPNEG	ADC data sampling edge selection on EOC: 0: ADC data is sampled on the rising edge of EOC. 1: ADC data is sampled on the falling edge of EOC. Note: This bit can only be set to 0 in the design of this chip.

15.2.6 ADC_DR0 Data Low Register

B6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_DR0	CHDATAL							
R/W	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	CHDATAL	A/D channel receive data low register

15.2.7 ADC_DR1 Data High Register

B7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_DR1	-	-	-	-	CHDATAH			
R/W	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	-	-
6:4	-	-
3:0	CHDATAH	A/D channel receive data high register

15.2.8 ADC_HL Channel Setting Register

F5H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_HL	-	ADCHL[6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	-	-
6:0	ADCHL	**ADCH[6:0] channel configuration bits:** ADCH[0]: 0: P1_4 is configured as GPIO. 1: P1_4 is configured as ADC input. ADCH[1]: 0: P1_5 is configured as GPIO. 1: P1_5 is configured as ADC input. ADCH[2]: 0: P2_0 is configured as GPIO. 1: P2_0 is configured as ADC input. ADCH[3]: 0: P2_2 is configured as GPIO. 1: P2_2 is configured as ADC input. ADCH[4]:

		0: P2_3 is configured as GPIO. 1: P2_3 is configured as ADC input. ADCH[5]: 0: P2_6 is configured as GPIO. 1: P2_6 is configured as ADC input. ADCH[6]: 0: P2_7 is configured as GPIO. 1: P2_7 is configured as ADC input.

15.2.9 ADC_CSTAT Start Register

F6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_CSTAT	-	-	-	-	-	-	-	RXAVL
R/W	R	R	R	R	R	R	R	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:1	-	-
0	RXAVL	● This signal indicates that BUF has received data. When RX BUF is not empty, this bit is 1. 1: RX BUF contains data. 0: RX BUF is empty. Writing 1 clears this bit. ● This signal facilitates CPU polling operations.

15.2.10 ADC_SPW Sampling Clock Pulse Width Configuration Register

F7H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_SPW	-	-	-	-	-	SAMPW		
R/W	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	1	1

Bit No.	Bit Designator	Description
7:3	-	-

2:0	SAMPW	Sampling clock pulse width configuration **Note:** In the design of this chip, this register must be programmed to a value ≥ 3. The valid value range of this register is 3–5, values beyond this range may cause abnormal ADC operation. 3: SMAPCLK width is 4 ADC_CLK pulse signals. 4: SMAPCLK width is 5 ADC_CLK pulse signals. 5: SMAPCLK width is 6 ADC_CLK pulse signals.

15.2.11 ADC_VREF Voltage Reference Source Selection Register

FDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_VREF	-	-	ADCSPEED		-	-	-	VREFSEL
R/W	-	-	R/W	R/W	-	-	-	R/W
Reset Value	-	-	0	0	-	-	-	0

Bit No.	Bit Designator	Description
7:6	-	-
5:4	ADCSPEED	ADCSPEED selection bits, reserved and kept at the default value 0
3:1	-	-
0	VREFSEL	ADC voltage reference selection bit: 0: V_{DDH} is used as the ADC voltage reference source. 1: External V_{REF} is used as the ADC reference source (when configured to 1, port P2_5 will serve as the external reference input).

15.2.12 ADC_CDR0 Clock Division Register

FEH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_CDR0	CLKDIV0							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	1	1	1	1	1	1	1	1

Bit No.	Bit Designator	Description
7:0	CLKDIV0	ADC internal clock division factor The ADC clock frequency formula is: $f_{adc\_clk} = f_{pclk}$ / {clkdiv1, clkdiv0} Wherein, f_{adc_clk} = frequency of ADC internal clock, f_{pclk} = frequency of

		APB clock, and clkdiv = clock division factor. Note: Do not set clkdiv to 0 or 1, otherwise, the division factor defaults to 2. If a 1-division is required, it is recommended to use an external clock.

15.2.13 ADC_CDR1 Clock Division Register

FFH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ADC_CDR1	CLKDIV1							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7:0	CLKDIV1	ADC internal clock division factor The ADC clock frequency formula is: $f_{adc\_clk} = f_{pclk}$ / {clkdiv1, clkdiv0} Wherein, f_{adc_clk} = frequency of ADC internal clock, f_{pclk} = frequency of APB clock, and clkdiv = clock division factor. Note: Do not set clkdiv to 0 or 1, otherwise, the division factor defaults to 2. If a 1-division is required, it is recommended to use an external clock.

15.3 Operation Process

15.3.1 Initialization

1. Configure ADCCEN of PCLK0 to 1 to enable the ADC clock.
2. Configure ADCREN of PRESET0 to 1 to release the ADC reset.
3. Configure ADCCLKSEL of ADCGCR0 to select the ADC clock source. If the clock generated by the internal clock divider is selected, configure ADCCDR0 and ADCCDR1 to set the division value of the divider.
4. Configure VREFSEL of ADCVREF to select the ADC voltage reference.

5. Configure SAMPW of ADCSPW to set the sampling clock pulse width.
6. Configure ADCHL to set the GPIO corresponding to the desired ADC channel as ADC input; if channel 0 is used as the sampling channel, configure P1_2_SEL of ADCGCR2 to select P1_2 or P1_4 as channel 0.
7. Configure ADCRCEN of ADCGCR0 to disable or enable read-clear of the ADC data register.
8. Configure ADCCUNSET of ADCGCR0 to select the operating mode of ADC.
9. Configure SAMPNEG of ADCGCR3 to 0 to sample on the rising edge of EOC.
10. Configure ADCPDEN of ADCGCR1 to 0 to power on the SAR ADC.
11. Configure ADCRST of ADCGCR1 to 0 to release the SAR ADC.
12. Configure ADCEN of ADCGCR0 to 1 to enable the ADC controller.
13. If ADC interrupt is required, configure IP0 and IP1 of IP to set the ADC interrupt priority.
14. Configure RXINTEN of ADCIER to 1 to enable the interrupt for valid data stored in the ADC RX BUF.
15. Configure EADC and EA of IEN0 to 1 to enable the ADC interrupt and the global interrupt.

15.3.2 Single-shot ADC Sampling

1. Configure CHEN of ADCGCR2 to enable the relevant ADC channel for analog-to-digital conversion.
2. Configure ADCSTEN of ADCGCR1: set the signal to 0 first and then to 1 to generate a low-to-high signal transition, thus the ADC conversion starts.
3. Read the status of ADCSTEN of ADCGCR1. When ADCSTEN is set to 0, the conversion is complete.
4. Read the status of RXAVL of ADCCSTAT. When RXAVL is set to 1, it means that there is data

in RXBUF. It shall be cleared by writing 1.

5. After the conversion is completed and the RX BUF contains data, read the channel data in ADCDR0 and ADCDR1.

6. In continuous mode, configure ADCEN of ADCGCR0 to 0 to stop the conversion.

15.3.3 Notes

1. The ADC sampling rate is set to 1 Msps, ADC sampling rate = f_{ADCCLK} / (sampling time + conversion time) = 16 MHz / (4clk + 12clk) = 1 Msps. When the clock generated by the system clock generator is selected as the clock source, the frequency division of ADCCDR0 and ADCCDR1 is invalid.

2. Channel 7 is the internal LDO channel.

16 LVD

16.1 Overview

The LVD module performs low-voltage detection. It can filter the detection results to improve system stability.

16.2 Register Description

Table 16-1: List of Registers

Address	Name	Description
DDH	LVD_CON	Enable register
A2H	OINTEN	Interrupt enable register
A3H	OINTUS	Interrupt status register
A6H	LVD_OSTATUS	Status register
D8H	LVD_RSTSTAT	Reset register
C004H	LVD_LV	Filter enable register

16.2.1 LVD_CON Enable Register

DDH	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LVD_CON	LVDF	-	LVDREN	LVDEN	LVDS[3:1]			-
RW	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value	0	0	0	0	0	0	0	0

Bit No.	Bit Designator	Description
7	LVDF	LVD detection status: 0: No low voltage detected 1: Low voltage detected
6	-	-
5	LVDREN	LVD reset enable control: 0: Disable low-voltage reset function 1: Enable low-voltage reset function (LVDEN must be set before

<table>
<tr><td></td><td></td><td>enabling reset)</td></tr>
<tr><td>4</td><td>LVDEN</td><td>LVD module enable control:
0: Enable LVD module
1: Disable LVD module</td></tr>
<tr><td>3:1</td><td>LVDS[3:0]</td><td>LVD point voltage settings:<table><tr><th>LVDS</th><th>LVD Point</th></tr><tr><td>000</td><td>4.39 V</td></tr><tr><td>001</td><td>3.95 V</td></tr><tr><td>010</td><td>3.59 V</td></tr><tr><td>011</td><td>3.29 V</td></tr><tr><td>100</td><td>3.04 V</td></tr><tr><td>101</td><td>2.82 V</td></tr><tr><td>110</td><td>2.63 V</td></tr><tr><td>111</td><td>2.46 V</td></tr></table></td></tr>
<tr><td>0</td><td>-</td><td>-</td></tr>
</table>

16.2.2 OINTEN Interrupt Enable Register

Please refer to Chapter “OINTEN Interrupt Enable Register” for details.

16.2.3 OINTUS Interrupt Status Register

Please refer to Chapter “OINTEN Interrupt Enable Register” for details.

16.2.4 LVD_OSTATUS Status Register

A6H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LVD_OSTATUS	-		BOOTLOCK	C_NVRLOCK	LVDLOW	NVR2LOCK	NVR1LOCK	EFCREADY
R/W	R	R	R	R	R	R	R	R
Reset Value	0	0	0	0	0	0	0	1

Bit No.	Bit Designator	Description
7:6	-	-
5	BOOTLOCK	BOOT area locked status: 1: BOOT area is locked. 0: BOOT area is not locked.

4	C_NVRLOCK	C_NVR area locked status: 1: C_NVR area is locked. 0: C_NVR area is not locked.
3	LVDLOW	Real-time LVD detection status: 0: LVD voltage is normal. 1: LVD voltage is too low.
2	NVR1LOCK	NVR1 area locked status: 1: NVR1 area is locked. 0: NVR1 area is not locked.
1	NVR0LOCK	NVR0 area locked status: 1: NVR0 area is locked. 0: NVR0 area is not locked.
0	EFCREADY	EFlash status indicator, reflecting the operating status of EFlash: 1: EFlash is idle. 0: EFlash is busy.

16.2.5 LVD_RSTSTAT Reset Register

D8H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LVD_RSTSTAT	WDOF	WDEN	LVDRF	PORF	ERSTF	WDT[2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset Value (POR)	0	0	x	1	x	0	0	0
Reset Value (WDT)	1	0	x	x	x	0	0	0
Reset Value (PIN)	x	0	x	x	1	0	0	0
Reset Value (LVD)	x	0	1	x	x	0	0	0

Bit No.	Bit Designator	Description
7	WDOF	Watchdog overflow flag bit: set to 1 by hardware when the watchdog overflows, and can be cleared by software or by power-on reset. 0: No WDT overflow occurred 1: WDT overflow occurred
6	WDEN	Watchdog enable bit: 0: Disable watchdog function 1: Enable watchdog function
5	LVDRF	LVD reset flag bit: set to 1 by hardware after LVD reset, and cleared by software.

		0: No low-voltage reset occurred 1: Low-voltage reset occurred
4	PORF	Power on reset flag bit: set to 1 by hardware after power-on reset, and cleared by software. 0: No power-on reset occurred 1: Power-on reset occurred
3	ERSTF	Pin reset flag bit: set to 1 by hardware after pin reset, and cleared by software. 0: No pin reset occurred 1: Pin reset occurred
2:0	WDT[2:0]	WDT overflow period control bit: 000: Minimum overflow period = 4096 ms 001: Minimum overflow period = 1024 ms 010: Minimum overflow period = 256 ms 011: Minimum overflow period = 128 ms 100: Minimum overflow period = 64 ms 101: Minimum overflow period = 16 ms 110: Minimum overflow period = 4 ms 111: Minimum overflow period = 1 ms

16.2.6 LVD_LV Filter Enable Register

C004H	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
LVD_LV	-	-	-	-	-	LVD_TSET		LVDLVEN
R/W	R	R	R	R	R	R/W	R/W	R/W
Reset Value	0	0	0	0	0	1	1	1

Bit No.	Bit Designator	Description
7:3	-	-
2:1	LVD_TSET	Filter time setting bits: 11: Filter time = 1 RC38K clock 10: Filter time = 8 RC38K clocks 01: Filter time = 16 RC38K clocks 00: Filter time = 29 RC38K clocks
0	LVDLVEN	LVD filter enable bit: 1: Enable RC38K clock filter function. 0: Disable RC38K clock filter function.

17 Interrupts

17.1 Main Features

- 7 interrupt sources: EX0, ES1, ES0, EPWM, EADC, EFC, SPI
- 4-level programmable interrupt priority

17.2 Interrupt Summary

Interrupt Source	Entry Address	Enable Bit	Flag Bit	Polling Priority	Interrupt Number (C Language)
Reset	0000H	-	-	0 (top priority)	-
INT0	0003H	EX0 + PxIENy	PxIRQy	1	0
UART1	0013H	ES1	RI1 + TI1	8	2
UART0	0023H	ES0	RI0 + TI0	12	4
PWM	002BH	EPWM + PWMxIE	PWMxIF	15	5
ADC	0033H	EADC + ADCIER	RXAVL	2	6
SPI	003BH	ESPI + SPIIE	SPI_SR	6	7
EFC	005BH	EFCINTEN + OINTEN	OINTUS	11	11
LPTIMER	0063H	LPTIMINTEN + LPTIE	LPTIMER_IF	14	12
I2C	006BH	I2CINTEN + I2CCR	-	17	13
UART2	0083H	UART2INTEN	UART_ISR	3	16
UART3	008BH	UART3INTEN	UART_ISR	7	17
GTIMER2	009BH	GTIMER2INTEN	GTIMER_SR	10	19
GTIMER1	00A3H	GTIMER1INTEN	GTIMER_SR	13	20
GTIMER0	00ABH	GTIMER0INTEN	GTIMER_SR	16	21

18 Instruction Set

The machine cycle is 1 clock cycle, and most instructions are completed within a single machine cycle.

18.1 Instruction Operand Notation

Rn	Working registers R0–R7
direct	256 internal RAM locations, any special function registers
@Ri	Indirect internal or external RAM location addressed by register R0 or R1
#data	8-bit constant included in instruction
#data 16	16-bit constant included as bytes 2 and 3 of instruction
bit	256 software flags, any bit-addressable I/O pin, control or status bit
A	Accumulator
addr16	Destination address for LCALL and LJMP may be anywhere within the 64K bytes of program memory address space
addr11	Destination address for ACALL and AJMP will be within the same 2K bytes page of program memory as the first byte of the following instruction
rel	SJMP and all conditional jumps include an 8-bit offset byte. Range is +127/-128 bytes relative to the first byte of the following instruction

18.2 Arithmetic Operation Instruction

Mnemonic	Description	Code	Byte	Cycle
ADD A, Rn	Add register to accumulator	28-2F	1	1
ADD A, direct	Add direct byte to accumulator	25	2	2
ADD A, @Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A, #data	Add immediate data to accumulator	24	2	2
ADDC A, Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A, direct	Add direct byte to A with carry flag	35	2	2
ADDC A, @Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A, #data	Add immediate data to A with carry flag	34	2	2
SUBB A, Rn	Subtract register from A with borrow	98-9F	1	1

Mnemonic	Description	Code	Byte	Cycle
SUBB A, direct	Subtract direct byte from A with borrow	95	2	2
SUBB A, @Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A, #data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

18.3 Logic Operation Instruction

Mnemonic	Description	Code	Byte	Cycle
ANL A, Rn	AND register to accumulator	58-5F	1	1
ANL A, direct	AND direct byte to accumulator	55	2	2
ANL A, @Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A, #data	AND immediate data to accumulator	54	2	2
ANL direct, A	AND accumulator to direct byte	52	2	3
ANL direct, #data	AND immediate data to direct byte	53	3	4
ORL A, Rn	OR register to accumulator	48-4F	1	1
ORL A, direct	OR direct byte to accumulator	45	2	2
ORL A, @Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A, #data	OR immediate data to accumulator	44	2	2
ORL direct, A	OR accumulator to direct byte	42	2	3
ORL direct, #data	OR immediate data to direct byte	43	3	4
XRL A, Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A, direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A, @Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A, #data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct, A	Exclusive OR accumulator to direct byte	62	2	3

Mnemonic	Description	Code	Byte	Cycle
XRL direct, #data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RL A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

18.4 Data Transfer Instruction

Mnemonic	Description	Code	Byte	Cycle
MOV A, Rn	Move register to accumulator	E8-EF	1	1
MOV A, direct	Move direct byte to accumulator	E5	2	2
MOV A, @Ri	Move indirect RAM to accumulator	E6:E7	1	2
MOV A, #data	Move immediate data to accumulator	74	2	2
MOV Rn, A	Move accumulator to register	F8-FF	1	2
MOV Rn, direct	Move direct byte to register	A8-AF	2	4
MOV Rn, #data	Move immediate data to register	78-7F	2	2
MOV direct, A	Move accumulator to direct byte	F5	2	3
MOV direct, Rn	Move register to direct byte	88-8F	2	3
MOV direct1, direct2	Move direct byte to direct byte	85	3	4
MOV direct, @Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct, #data	Move immediate data to direct byte	75	3	3
MOV @Ri, A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri, direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri, #data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR, #data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A, @A+PC	Move code byte relative to PC to accumulator	83	1	3
MOVX A, @Ri	Move external RAM (8-bit address) to A	E2-E3	1	3-10
MOVX A, @DPTR	Move external RAM (16-bit address) to A	E0	1	3-10
MOVX @Ri, A	Move A to external RAM (8-bit address)	F2-F3	1	4-11
MOVX @DPTR, A	Move A to external RAM (16-bit address)	F0	1	4-11

Mnemonic	Description	Code	Byte	Cycle
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A, Rn	Exchange register with accumulator	C8-CF	1	2
XCH A, direct	Exchange direct byte with accumulator	C5	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A, @Ri	Exchange low-order nibble indir.RAM with A	D6-D7	1	3

18.5 Control Program Jump Instruction

Mnemonic	Description	Code	Byte	Cycle
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LIMP addr16	Long jump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A + DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit, rel	Jump if direct bit is set	20	3	4
JNB bit, rel	Jump if direct bit is not set	30	3	4
JBC bit, direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A, direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A, #data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn, #data rel	Compare immediate to register and jump if not equal	B8-BF	3	4
CJNE @Ri, #data rel	Compare immediate to indirect and jump if not equal	B6-B7	3	4
DJNE Rn, rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct, rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

18.6 Bitwise Operation Instruction

Mnemonic	Description	Code	Byte	Cycle
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C, bit	AND direct bit to carry flag	82	2	2
ANL C, /bit	AND complement of direct bit to carry	B0	2	2
ORL C, bit	OR direct bit to carry flag	72	2	2
ORL C, /bit	OR complement of direct bit to carry	A0	2	2
MOV C, bit	Move direct bit to carry flag	A2	2	2
MOV bit, C	Move carry flag to direct bit	92	2	3

19 Power Supply Scheme

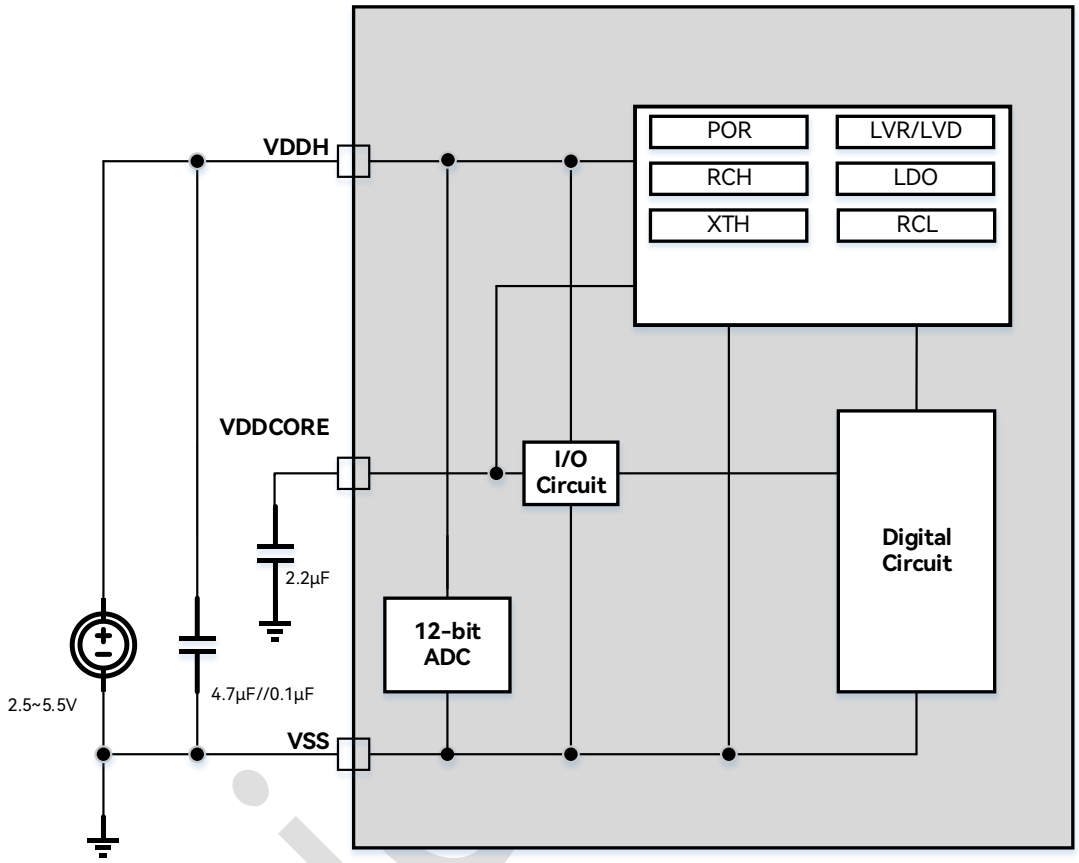


Figure 19-1: Power Supply Scheme Diagram

20 Revision History

Version	Date	Modifications
V1.0	Mar-20-2025	Initial release.
V1.0.1	May-12-2025	Updated Figure 19-1: Power Supply Scheme Diagram.
V1.0.2	Jun-06-2025	Remove the words “Temperature drift” from bits 7:4 in “4.1.31 RCHTRIML”.

