UNICMICRO 广芯微电子

UM32Mx56

32-bit Motor Control MCU: ARM®Cortex®-M0+, 32KB eFlash, 6KB SRAM

Product Features

TSSOP28 (9.7*4.4 mm) SSOP24 (8.6*3.9 mm) QFN40 (5*5 mm)

- **Power management system**
  - Built-in ROSC/LDO/POR, no crystal/ LDO/ reset circuits required
- **Processor**
  - 32-bit ARM Cortex-M0+, up to 60 MHz
  - Single-cycle hardware multiplier
  - Chip-integrated advanced Prefetch instruction accelerator, featuring industry-leading instruction execution efficiency
  - Supporting interrupt remapping function
- **Memory**
  - 6KB SRAM
  - 32KB eFlash:
    - ✓ Sector size: 512 B
    - ✓ Endurance: 100,000 cycles
    - ✓ Data retention time: 100 years @ room temperature
  - 4KB EEPROM
    - ✓ EEPROM data will not be overwritten during eFlash erasing/writing
- **GPIO**
  - Up to 26 I/O ports with interrupt capability
  - Configurable drive capability: 16 mA/8 mA
- **Clocks**
  - Internal high-speed clock: 60 MHz
  - Internal low-speed clock: 32.768 kHz
- **Communication interfaces**
  - 2 × UARTs
  - 1 × SPI: supporting master/slave modes, Mode 0/1/2/3 protocols, with a maximum rate of 16 Mbps, master mode supporting three-wire mode and multiple-chip selection
  - I2C: supporting master/slave modes, with rates of 100 kbps/400 kbps/1 Mbps
- **Analog peripherals**
  - ADC: 16 channels (11 external, 5 internal), 12-bit resolution, 1.2Msps sampling rate, supporting channel injection, full/semi-automatic modes, and hardware trigger function. Input channels are equipped with maskable enhanced driver buffers.
  - PGA: 3 operational amplifiers, supporting differential input, with gain programmable from 1 to 64 times, and can be cascaded with the ADC inside the chip.
  - COMP: 2 voltage comparators, supporting hardware polling between comparison channels, detecting rising edge, falling edge and both edges of comparison results, as well as multiple filtering modes for comparison results.
  - VREF: Built-in independent analog voltage reference source with multiple configurable voltage levels.
- **Timers**
  - 1 x 32-bit GTimer, 2 x 16-bit GTimers, 12-channel PWM output, input capture, output compare, supporting incremental quadrature encoder and Hall sensor
  - 1 x 32-bit LPTimer, supporting 2-channel PWM output and 2-channel input capture
  - 1 × 16-bit ATimer, supporting 4-channel input capture, 3-channel dead-time complementary PWM output, and 1-channel PWM output; with hardware phase-shift function, and can set 2-channel ADC

hardware triggers
  - 1 x 32-bit low-power WDT, resettable and interruptible
  - 1 x 18-bit WWDT, resettable and interruptible

- **Security**
  - SWD read protection, and physical disable feature to prevent eFlash program theft
  - eFlash data encryption, ECC error correction, and anti-erase/write functions to enhance system operation security
  - Hardware acceleration for the CRC16-CCITT data verification algorithm
  - Low-voltage detection (LVD), monitoring supply voltage
  - Low-voltage reset (LVR), anti-crash
  - 16-byte UUID
  - Built-in hardware true random number generator

- **Hardware arithmetic acceleration engine**
  - Built-in hardware divider, providing results within 8 system clock cycles
  - Built-in square root operation hardware accelerator, providing results within 4 system clock cycles

- **Electrical paramters**
  - Operating voltage: 2.3 V–5.5 V
  - Operating temperature: -40℃–105℃

- **Moisture sensitivity level:** MSL-3

- **Development support**
  - JTAG->SWD mode for online debugging/downloading
  - SDK development kit, EVB development board
  - Off-line programmer

- **Device summary**

Type	Part No.
32 KB	UM32M156-G6P7 (TSSOP28)
	UM32MP56-E6P7 (SSOP24)
	UM32MP56-H6U7 (QFN40)

Contents

1 Product Introduction

The UM32Mx56 series of chips are 32-bit motor processor SoC chips developed by Unicmicro based on the ARM Cortex-M0+ core. These chips are designed with a low pin count and wide voltage operating range, targeting a variety of application scenarios including industrial equipment and motor control. According to the specific application requirements of the industry, the chip integrates general-purpose peripheral communication interfaces (including 12-bit SAR ADC, UART, SPI, I2C, etc.), sensor acquisition interfaces (including ADC, PGA, COMP, etc.), low-power module interfaces (including LPTIMER, WDT, etc.), and hardware algorithm modules (including SQRT for square root calculations, DIV for division, etc.). The chips feature high integration, high interference immunity, and high reliability. They have built-in RC oscillators of both high frequency and low frequency, supporting crystal-free applications. They support the Keil MDK integrated development environment and software development in C language and assembly language.

The UM32Mx56 series chips have enhanced security features, including anti-theft mechanisms for data protection, SWD read protection, and physical disabling of the SWD interface. The internal eFlash memory of the chip has been enhanced with ECC error correction codes and data encryption functions. ECC error correction can effectively prevent data loss in eFlash or occasional read errors due to environmental factors. In addition, the chip has implemented a protection mechanism against erasure and rewriting for certain EEPROM areas and the 32KB eFlash main storage area, effectively preventing customer application data and programs from being rewritten.

Applications:

- Industrial applications
- Motor applications
- Intelligent transportation, smart cities, smart homes

1.1 Functional Block Diagram

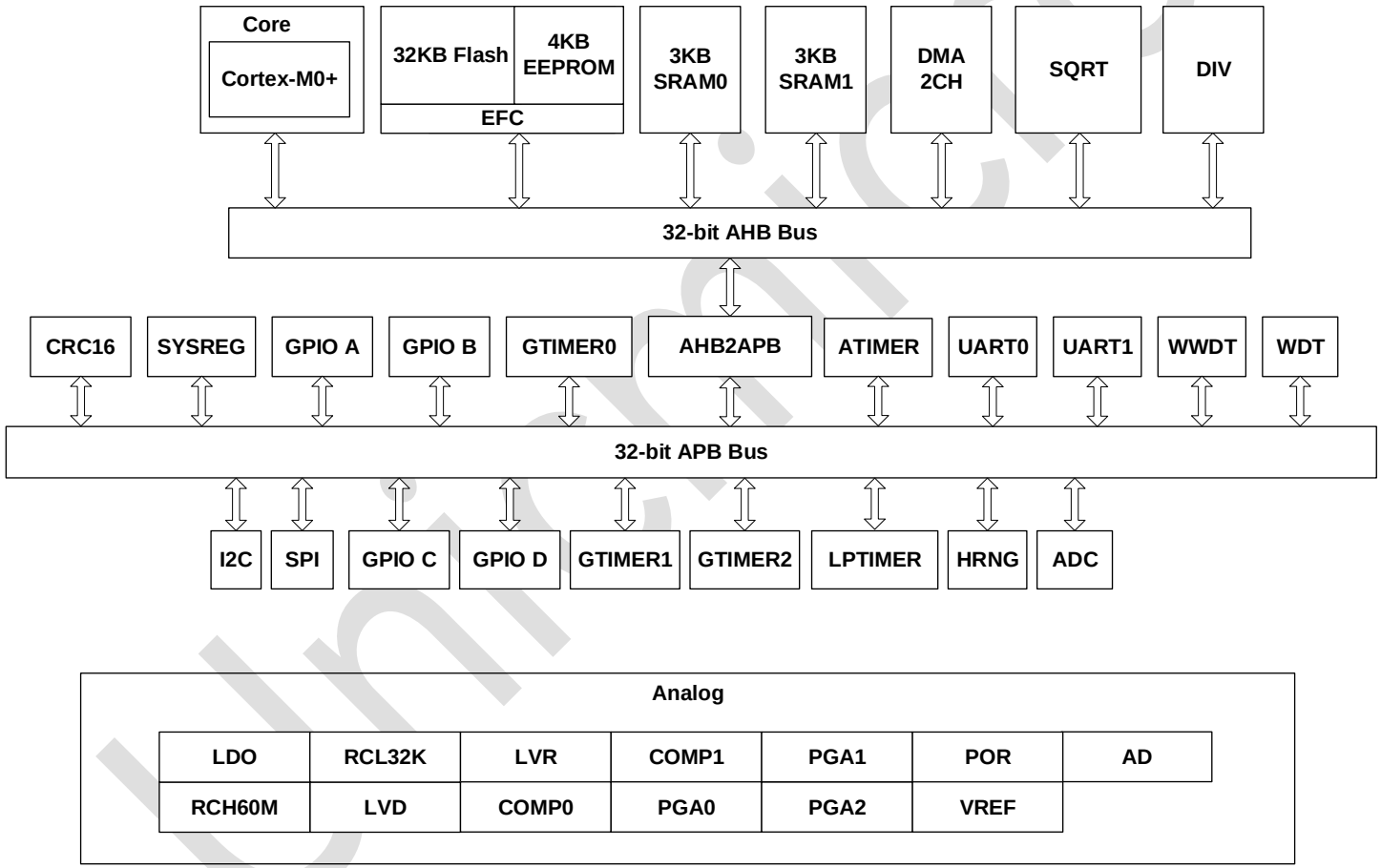


Figure 1-1: Functional Block Diagram

1.2 Naming Convention

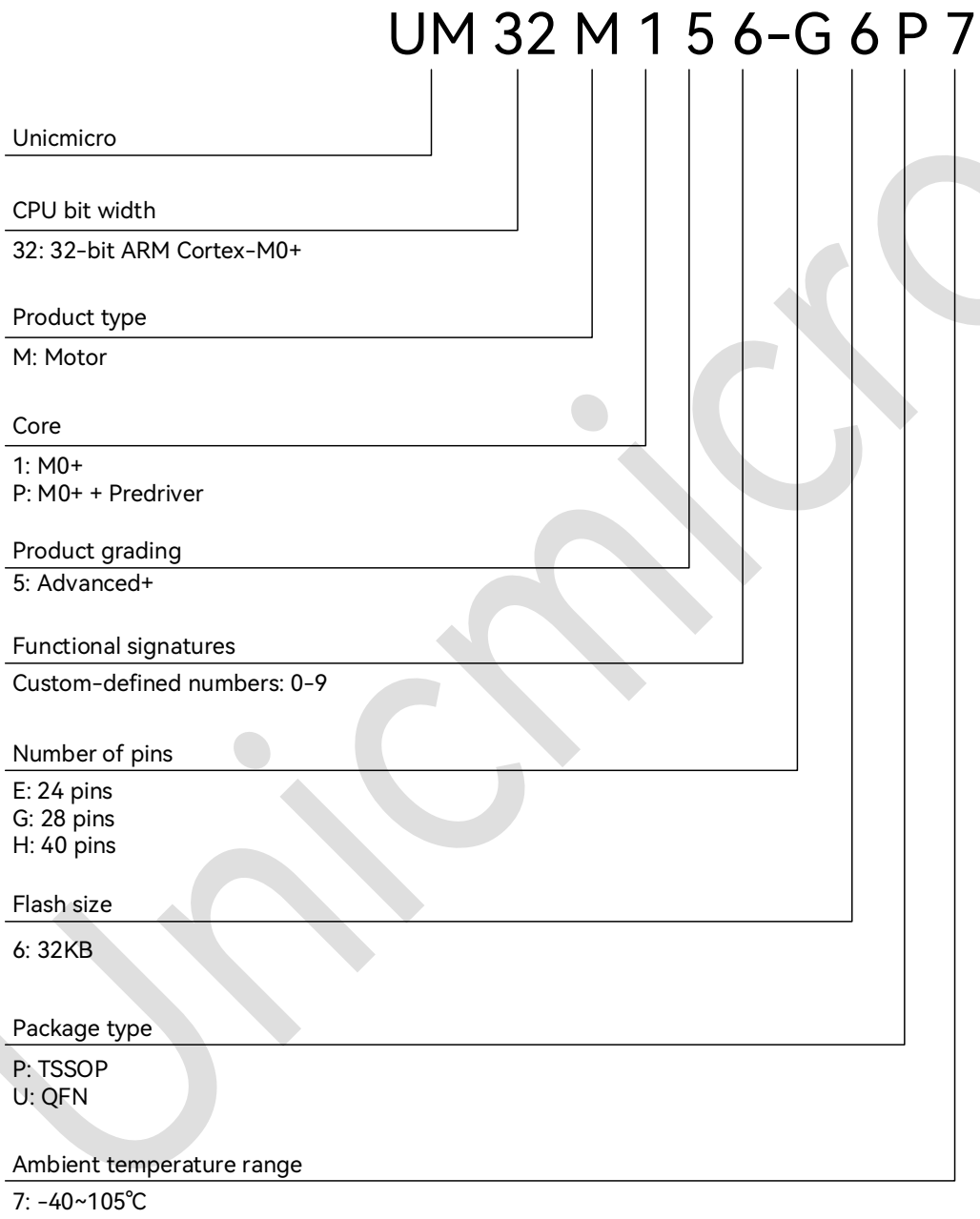


Figure 1-2: Schematic Diagram of Naming Convention

1.3 Configuration Table

Table 1-1: Configuration Table

Part No.		UM32MP56-E6P7	UM32MP56-H6U7	UM32M156-G6P7
Flash (KB)		32		
EEPROM (KB)		4		
SRAM (KB)		6		
DMA Channels		1 2		
SIP	Pre-driver	3P + 3N	6N	No
	LDO	5 V	5 V + 12 V	No
	Pre-driver supply voltage	5 V–28 V	5 V–20 V	No
	Drive power withstand voltage	40 V	70 V	No
Timer	General-purpose timers	2 (16-bit), 1 (32-bit)		
	Advanced control timer	1 (16-bit)		
	SysTick	Yes		
	WDT	1		
	WWDT	1		
	LPTIMER	1		
	PWM channels	14	21	21
Communication interfaces	SPI	1		
	I2C	1		
	UART	2		
GPIO		14	20	26
Analog	12-bit ADC Channels	1 16		
	PGA	3		
	COMP	2		
Hardware acceleration engine	CRC	Yes		
	SQRT	Yes		
	DIV	Yes		
	True random number generator	Yes		
Maximum operating frequency		60 MHz		

Part No.	UM32MP56-E6P7	UM32MP56-H6U7	UM32M156-G6P7
Operating voltage	2.3 V–5.5 V		
Operating temperature	Ambient temperature: -40℃–+105℃		
	Junction temperature: -40℃–+110℃		
Package	SSOP24	QFN40	TSSOP28

2 Functional Overview

2.1 Core

The Cortex™ M0+ processor is a 32-bit two-stage pipeline RISC processor embedded with an AMBA-Lite interface and a nested vectored interrupt controller (NVIC). It features hardware debugging function, Thumb instruction execution and compatibility with other Cortex-M series processors. The processor also incorporates a number of brand-new designs as well as energy-saving and consumption-reducing technologies to improve debugging and tracing capabilities, reduce the number of instructions per cycle (IPC), and improve the two-stage pipeline for Flash access. The Cortex M0+ fully supports the integrated Keil & IAR debuggers.

2.2 Memory

The chip integrates embedded eFlash and embedded SRAM.

2.2.1 Embedded Flash

The chip embeds a 32KB eFlash for storing programs and data.

2.2.2 Embedded SRAM

The on-chip 6KB SRAM allows to maintain data in STOP mode.

2.3 Chip Data Security Protection

- SWD hardware protection

  By configuring the keyword “SWD_DISABLE_PIN” in the EEPROM, the SWD interface is hardware-disabled, prohibiting communication through the SWD interface, thereby preventing physical access or illegal debugging via the SWD interface, safeguarding against malicious code injection or firmware tampering. Once the SWD hardware protection function is enabled, it is irreversible.

- SWD read protection

  By configuring the keyword “SWD_READ_DISABLE” in the EEPROM, read operations on the eFlash memory through the SWD interface are prohibited, protecting firmware code and sensitive data from being extracted. Customers can only unlock read operations on the eFlash in this power-on cycle by erasing the main area of the eFlash.

- eFlash sector write protection

  The eFlash memory is managed in partitions, and write protection for data in different areas is achieved by configuring the keyword “OTP_MAIN_EN” in the EEPROM.

- ECC function

  Error-correcting code technology is used to detect and correct read data errors in eFlash memory cells, ensuring data integrity and preventing read data corruption caused by hardware aging or environmental interference.

- EEPROM sector write protection

  The EEPROM storage space is managed in partitions, and erase/write protection for data in different areas is achieved by configuring the keywords “OTP_EEP0_EN”, “OTP_EEP1_EN”

and “OTP_EEP2_EN” in the OTP. Once the OTP keywords are enabled, the values in the corresponding EEPROM areas cannot be rewritten, including keywords such as SWD_READ_DISABLE, SWD_DISABLE_PIN, and OTP_MAIN_EN.

2.4 Nested Vectored Interrupt Controller (NVIC)

The nested vectored interrupt (NVIC) is a key component of Cortex-M0+. It is tightly coupled with the CPU processor core to achieve low interrupt latency and effective handling of new incoming interrupts, which are prioritized by NVIC connecting the external interrupt signals.

Cortex-M0+ embeds an NVIC which is able to handle up to 21 interrupt request (IRQ) inputs with 4 priority levels, to handle complex logic, as well as to perform real-time control and realize interrupt processing.

All NVIC registers can only be accessed using word transfers. Any attempt to read/write half-words or bytes will result in unpredictable behavior.

This module provides flexible interrupt management with minimal interrupt latency.

2.5 Clock Architecture

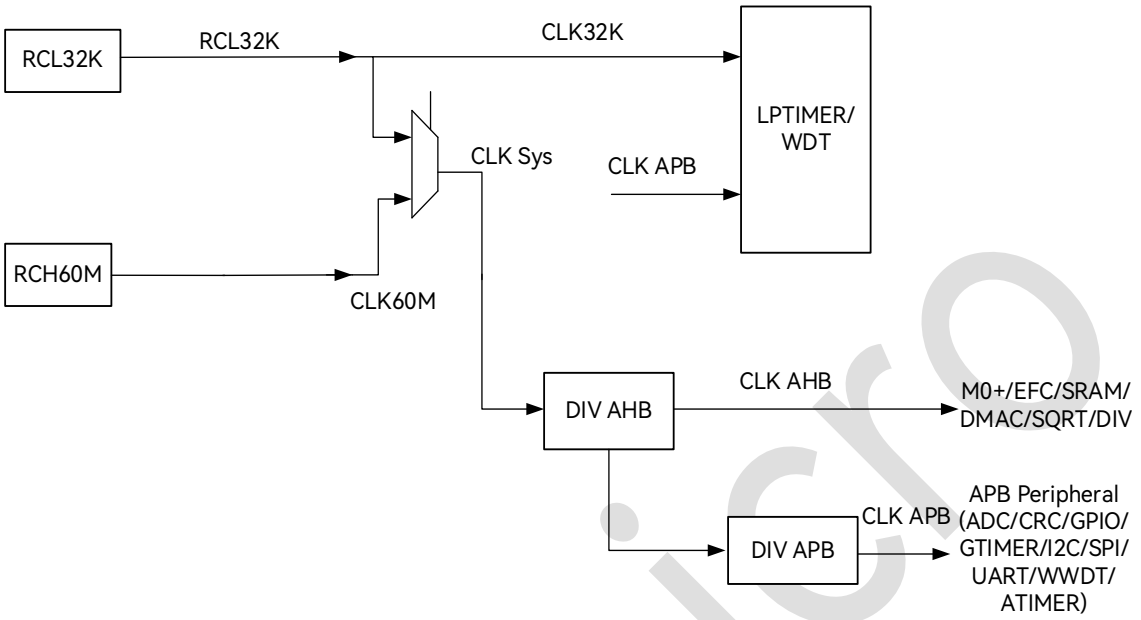


Figure 2-1: Clock Architecture Diagram

The system has two clock sources:

- 60 MHz high-precision internal clock (RCH), serving as system clock source
- 32 kHz internal RCL, serving as low-power clock and can be used as system clock source

Different clock schemes are required for different operation modes. The system clock source can be selected via configuring the CLK_SEL bit [14] in the system control register 0 (SYSCTRL0). The relationship is shown in the table below:

Table 2-1: System Clock Selection

CLK_SEL	System Clock Source
0	RCH
CLK_SEL	**System Clock Source**
1	RCL

2.6 Reset

The system reset sources are listed below.

Table 2-2: System Reset Sources

Reset Source	Description
Internal analog POR	Reset everything
LVR	
RESETEN	Reset everything except the CPU DEBUG logic
LOCKUP Reset	Reset logic other than EFC
LVD Reset	
WDT	
WWDT	
SOFT_RESETN	
Module reset	Reset the corresponding IP modules

2.7 Operating Mode

In addition to the normal operating mode, the chip provides three low-power modes to reduce its current consumption: Sleep mode, DeepSleep mode, and Stop mode.

Table 2-3: Low-power Modes Summary

Mode	Mode Description	Entry Condition	Exit Condition
Sleep	Powered by LDO Active, the CPU is mostly in sleep mode (including NVIC), while WIC is not in sleep mode; software can disable the clocks of various modules.	1. Disable the clocks of peripheral modules as required, leaving only those needed for monitoring interrupt events. 2. Execute WFI/WFE instructions.	1. CM0+ detects an interrupt or event. 2. Enter the interrupt service routine to clear the interrupt and return. 3. Continue executing subsequent instructions.

Mode	Mode Description	Entry Condition	Exit Condition
DeepSleep	Powered by LDO Standby, the CPU is mostly in sleep mode (including NVIC), while WIC is not in sleep mode; the high-speed clock source is disabled, and the RCL low-speed clock source is running.	1. Disable the clocks of peripheral modules as required, leaving only those needed for monitoring interrupt events. 2. Set the DeepSleep register inside CM0+. 3. Execute WFI/WFE instructions.	1. CM0+ detects an interrupt or event. 2. Enter the interrupt service routine to clear the interrupt and return. 3. Continue executing subsequent instructions.
Stop	Powered by LDO Standby, all system clocks are disabled.	1. Set the conditions for IO wake-up as required. 2. Set the DeepSleep register inside CM0+. 3. Set the STOPMODE_SEL register in system register. 4. Execute WFI/WFE instructions.	1. An external IO wake-up event occurs. 2. CM0+ detects the interrupt triggered by external IO wake-up event. 3. Enter the interrupt service routine to clear the interrupt and return. 4. Continue executing subsequent instructions.

2.8 Direct Memory Access Controller (DMA)

Direct memory access (DMA) supports 2-channel data transfer. The DMA is used to provide high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions, which keeps the CPU resources free for other operations, thus improving the system efficiency.

Main features:

- Capable of controlling data transfer between SRAM, SPI, UART0, UART1, ADC, LPTIMER,

ATIMER, GTIMER0, GTIMER1, and GTIMER2 modules

- Supporting memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral modes
- Internally provided with 2 DMA channels
- Configurable bit width and block length of data transfer
- Maximum block length: 32767 words
- Supporting fixed and incremental transfers for both source address and destination address
- Supporting infinite transfer
- Supporting burst transfer, with configurable transfer numbers ranging from 2 to 9

2.9 Universal Asynchronous Receiver Transmitter (UART)

UART supports full-duplex communication. It serially transmits data that is parallel-transmitted from memory or a processor to the UART receiver of a peripheral, or receives serial data from a UART peripheral and converts it into parallel data for the processor. UART supports serial communication with external interface devices.

The chip embeds two UART modules: UART0 and UART1.

Main features:

- Providing standard asynchronous communication bits (start bit, parity bit, stop bit):
  - Generating 1 start bit
  - Supporting 8-bit data width

- Generating 1 parity bit (odd or even), or no parity bit
- Generating 1 or 2 stop bits
- Bytes transmitted sequentially from LSB to MSB

- Programmable baud rate
- Supporting transfer at common baud rates such as 9600 bps, 19200 bps and 115200 bps

2.10 General-purpose Input/Output Interface (GPIO)

GPIO contains general-purpose data input/output interfaces, which can be shared with other functional pins, depending on the chip configuration. With these data interfaces, any number of pins can be configured as interrupt signals. The chip is provided with four groups of GPIOs, namely GPIOA, GPIOB, GPIOC and GPIOD, which can be abbreviated as PA, PB, PC and PD respectively. The GPIO registers shall set corresponding bits for their functions. For example, to set the direction of PA1 as output, the control bit[1] of GPIO_DIR shall be set to 1, and the settings of other bits follow this principle, that is, the direction of PAx can be set via the corresponding control bit[x] of GPIO_DIR.

Main features:

- The direction of any I/O port can be configured by software.
- Each GPIO_IN pin can be configured to trigger an interrupt in edge or level mode.
- Hardware filtering function for GPIO is supported.

2.11 Advanced Timer (ATIMER)

The advanced timer contains a 16-bit auto-reload counter and a programmable prescaler that

can support multiple applications such as input capture, output compare, PWM, complementary PWM with dead-time insertion, etc.

Main features:

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing real-time adjustment of the counter clock division
- 4 independent channels for input capture, output compare, PWM generation, and one-pulse output
- Complementary output with programmable dead-time insertion
- Supporting cascading between timers
- Repetition counter, supporting timer state update after multiple cycles
- Break input pins, comparator break, SVD break, break signal filtering and polarity selection, and combinatorial configuration of break signals
- Interrupt or DMA events can be generated on the following occurrences:
  - Counter overflow/underflow, counter initialization (software or hardware trigger)
  - Trigger events (counter start, stop, initialization, internal/external trigger)
  - Input capture
  - Output compare
  - Break signal input
- Supporting incremental quadrature encoder and Hall sensor
- Supporting phase-shift function

2.12 General-purpose Timer (GTIMER)

There is a 32-bit general counter GTIMER0 and two 16-bit general counters GTIMER1/2, each with its own independent interrupt. These timers can be used for various purposes, including measuring the pulse width of input signal (input capture) or generating output waveform (PWM, complementary PWM with dead-time insertion). The counter can count up, down or both up and down with the counter value accessible by software at any time.

GTIMER0 main features:

- 32-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing real-time adjustment of the counter clock division
- 4 independent channels for input capture, output compare, PWM generation, and one-pulse output
- Support cascading with other timers
- Interrupt or DMA events can be generated on the following occurrences:
  - Counter overflow/underflow, counter initialization (software or hardware trigger)
  - Trigger events (counter start, stop, initialization, internal/external trigger)
  - Input capture
  - Output compare
- Supporting incremental quadrature encoder and Hall sensor

GTIMER1/2 main features:

- 16-bit up, down, up/down auto-reload counter

- 16-bit programmable prescaler allowing real-time adjustment of the counter clock division
- 4 independent channels for input capture, output compare, PWM generation, and one-pulse output
- Support cascading with other timers
- Interrupt or DMA events can be generated on the following occurrences:
  - Counter overflow/underflow, counter initialization (software or hardware trigger)
  - Trigger events (counter start, stop, initialization, internal/external trigger)
  - Input capture
  - Output compare
- Supporting incremental quadrature encoder and Hall sensor

2.13 Low-power Timer (LPTIMER)

The LPTIMER is a 32-bit low-power timer/counter module. Due to the variety of its clock sources, it can remain operational with extremely low power consumption. The LPTIMER can operate without an internal clock, enabling external pulse counting in sleep mode. It can also work in conjunction with external trigger signals to achieve low-power timeout wake-up.

Main features:

- Independent 32-bit up counter
- 3-bit asynchronous clock prescaler with 8 division factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable operating clocks:
  - Internal clock source: LSCLK (CLK32K), RCLP (CLK1HZ), PCLK

  - External clock source: LPTIN (with analog filter)

- 32-bit compare/capture register
- 32-bit target value register
- Continuous/single-shot trigger mode
- Configurable input polarity
- External pulse counting without clock
- Sleep timeout wake-up triggered by external signal
- PWM output

2.14 Inter-integrated Circuit (I2C) Interface

The I2C bus interface connects the microcontroller to the serial I2C bus. The I2C module is responsible for receiving and transmitting data, as well as converting data between serial and parallel formats. It is connected to the I2C bus via the data line SDA and the clock line SCL, controlling all the I2C bus-specific sequencing. This module supports both master and slave modes.

Main features:

- Standard mode (100 Kb/s) / fast mode (400 Kb/s) / fast mode+ (1 Mb/s)
- 7-bit and 10-bit addressing modes
- Interrupt polling function
- Low-power slave design, capable of receiving data without a system clock
- Supporting asynchronous slave address matching wake-up, data frame reception completion wake-up, or START detection wake-up.

2.15 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a serial synchronous communication means for external devices to exchange data over a single line. The chip provides one SPI module that can be configured as a master or slave device to enable SPI communication with the outside.

Main features:

- Full-duplex or half-duplex single-data-line serial synchronous transfer
- Master and slave modes
- Programmable clock polarity and phase (supporting modes 0/1/2/3)
- Programmable bit rate
- Maximum frequency: $f_{sys}/2$
- Transfer complete interrupt flag
- Write conflict error flag
- Error detection, protection and interrupt flags in master mode
- Supporting DMA
- 8-byte deep FIFO

2.16 Independent Watchdog Timer (WDT)

The watchdog timer can generate a non-maskable interrupt or a reset when it reaches the given timeout value. It can be used to regain control when the system fails to respond as expected due to software errors or external device failures.

Main features:

- 32-bit down-counter with programmable load
- Independent watchdog timer enable
- Interrupt generation logic with interrupt masking
- Software runaway protection lock register
- Software boot function: reset enabling / disabling in WDT control register
- The register configuration of timer counting can be suspended when the CPU is suspended during debugging.

2.17 System Window Watchdog (WWDT)

The window watchdog timer (WWDT) is a watchdog running synchronously with CPU, aiming at monitoring the operating status of CPU in real time, so that it can reset CPU in the case of abnormal operation to avoid unpredictable consequences.

Main features:

- 18-bit upcounter with programmable load
- Internal fault detector of the system
- Clock synchronized with the system clock
- Reset will be triggered if the watchdog is fed before the window or not fed within the timeout period (the valid window for feeding the watchdog is 50%-100% of the time)
- An early warning interrupt will be triggered when the counter reaches 75% of the overflow time.

2.18 Random Number Generator (RNG)

RNG refers to the random number generator that is capable of delivering random number sequences by writing different random seeds.

2.19 Divider (DIV)

The implementation goal of DIV is to support division operations with divisors not exceeding 32 bits.

Main features:

- Signed integer operations
- Supporting divisions with divisors not exceeding 32 bits
- Division-by-zero warning function
- Output the calculation result within 8 AHB clock cycles

2.20 Analog-to-digital Converter (ADC)

The 12-bit successive approximation ADC with up to 16 input channels can measure signals from 11 external sources, 1 internal VREF output, 1 internal 1/4 VDDH output, 1 PGA0 output, 1 PGA1 output, and 1 PGA2 output. The A/D conversion of these channels can be performed in either single-shot or continuous scan mode. The ADC controller facilitates the communication between CPU and SAR ADC. The result of ADC conversion is stored in the lower 12 bits of the data register.

Main features:

- Supporting DMA transfer mode
- 5-bit programmable divider for generating the A/D clock
- Input channels with buffer function, enabling the input channel buffer driver
- 12-bit resolution A/D input data, with a maximum sampling rate of 1.2 MSPS (configurable via software)
- 16-channel ADC input: 11 external pin channels, 3 internal PGA outputs, 1 internal VREF input, and 1 internal 1/4 VDDH input
- Analog ADC can be disabled
- Polling and interrupt transfer modes
- Supporting single-shot scan or continuous scan modes, as well as semi-automatic or full-automatic scan modes
- Interrupt sources: single conversion complete interrupt, conversion sequence complete interrupt, injected channel single conversion complete interrupt, injected channel conversion sequence complete interrupt, analog watchdog upper limit exceed interrupt, analog watchdog lower limit drop interrupt, data conflict interrupt; channel data valid flags (one flag for each of the 8 regular channels, 4 injected channels, and oversampling)
- Supporting on-chip peripheral-triggered ADC conversion
- ADC voltage input range: 0–V_{REF}
- Optional reference voltage source: chip power supply voltage V_{DDH}, external voltage of IO pin V_{REFIO}

2.21 Programmable Gain Amplifier (PGA)

The device includes three programmable gain amplifiers (PGAs). The voltage gain of the three PGA channels is programmable from 1 to 64 times, and the output common-mode voltage can be programmed via software. The outputs of the three PGAs can be connected to PAD outputs via switches.

Main features:

- Built-in 3-channel PGA circuits
- Programmable gain: 1, 2, 4, 8, 16, 32, 64
- Input offset voltage can be trimmed
- Negative input terminal can be internally grounded
- Programmable output common-mode voltage: V_{REF}, V_{BG}
- Output can be connected to PAD via switch

2.22 Analog Comparator (COMP)

COMP is a comparator with rail-to-rail input and adjustable hysteresis. It features a multi-channel input switch that allows selection of different input signals.

Main features:

- 2 x voltage comparators
- Capable of generating comparison interrupts
- Supporting hardware polling between comparison channels

- Supporting detection of rising edge, falling edge and both edges of comparison results, with four comparison result filtering modes
- Built-in DAC for generating comparison voltage

2.23 Voltage Reference (VREF)

VREF is a voltage reference source that requires no external capacitors. It can output voltages of 1.2 V / 3.6 V / 4.2 V, or VDDH to serve as a voltage reference for analog circuits.

Main features:

- Selectable and configurable output voltages: 1.2 V, 3.6 V, 4.2 V, and VDDH.

2.24 Security System

2.24.1 UID

Each chip is shipped with a unique 16-byte device identifier, including wafer lot information, chip coordinate information, etc.

2.24.2 CRC16 Hardware Cyclic Redundancy Check

CRC16 is a hardware 16-bit CRC cyclic redundancy check calculation circuit based on the polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$. It can calculate the appropriate CRC result based on the user-preset CRC initial value and communication data, and supports setting the direction (forward and reverse) of input data and results.

2.25 Debugging and Programming System

The embedded debugging solution provides a full-featured real-time debugger, compatible with standard and mature debugging and development software such as Keil/IAR, supporting 4 hardware breakpoints and multiple software breakpoints.

3 Pin Definition and Description

3.1 Pin Definition

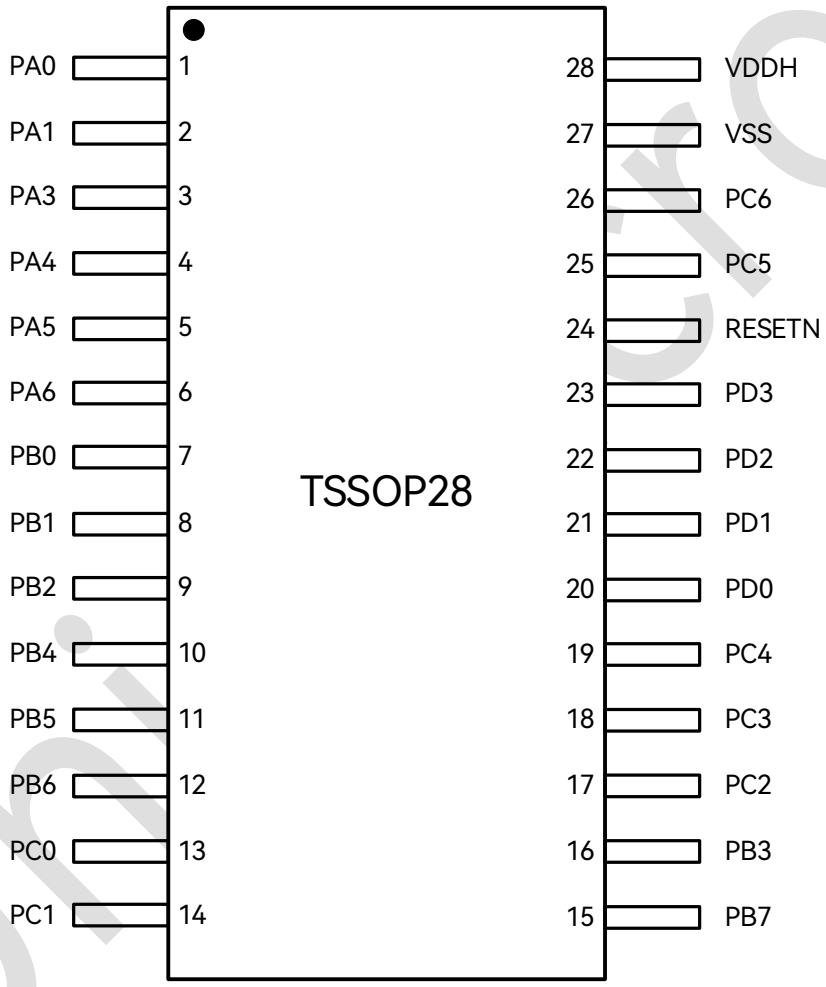


Figure 3-1: UM32M156-G6P7 Pinout Diagram

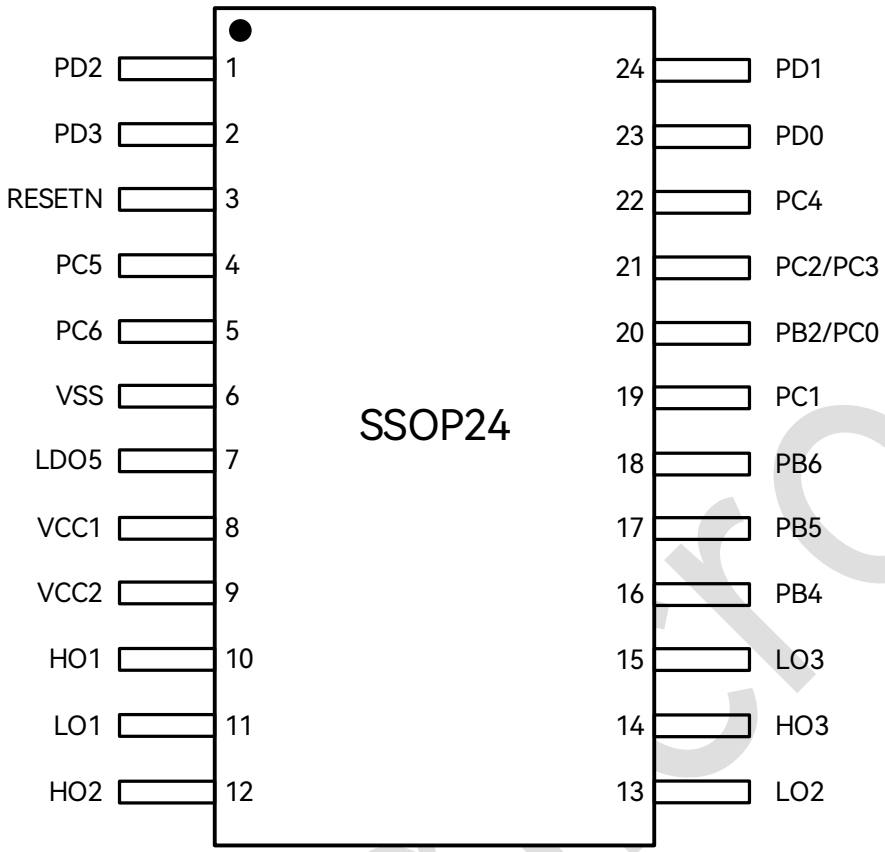


Figure 3-2: UM32MP56-E6P7 Pinout Diagram

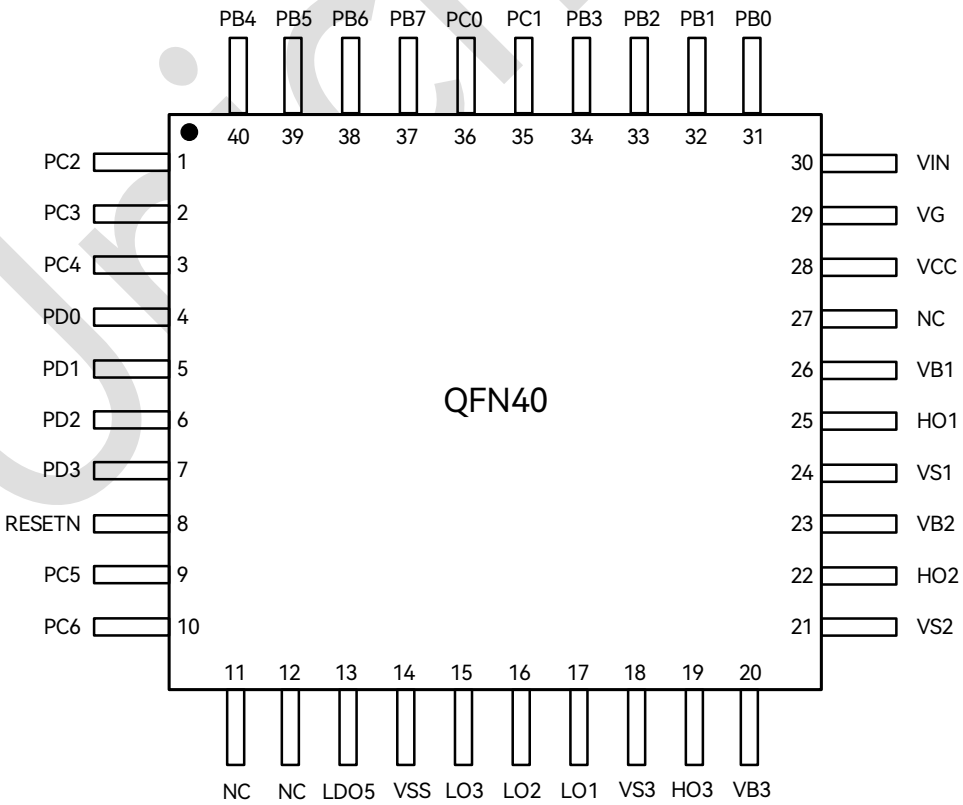


Figure 3-3: UM32MP56-H6U7 Pinout Diagram

3.2 Block Diagram

3.2.1 UM32M156-G6P7

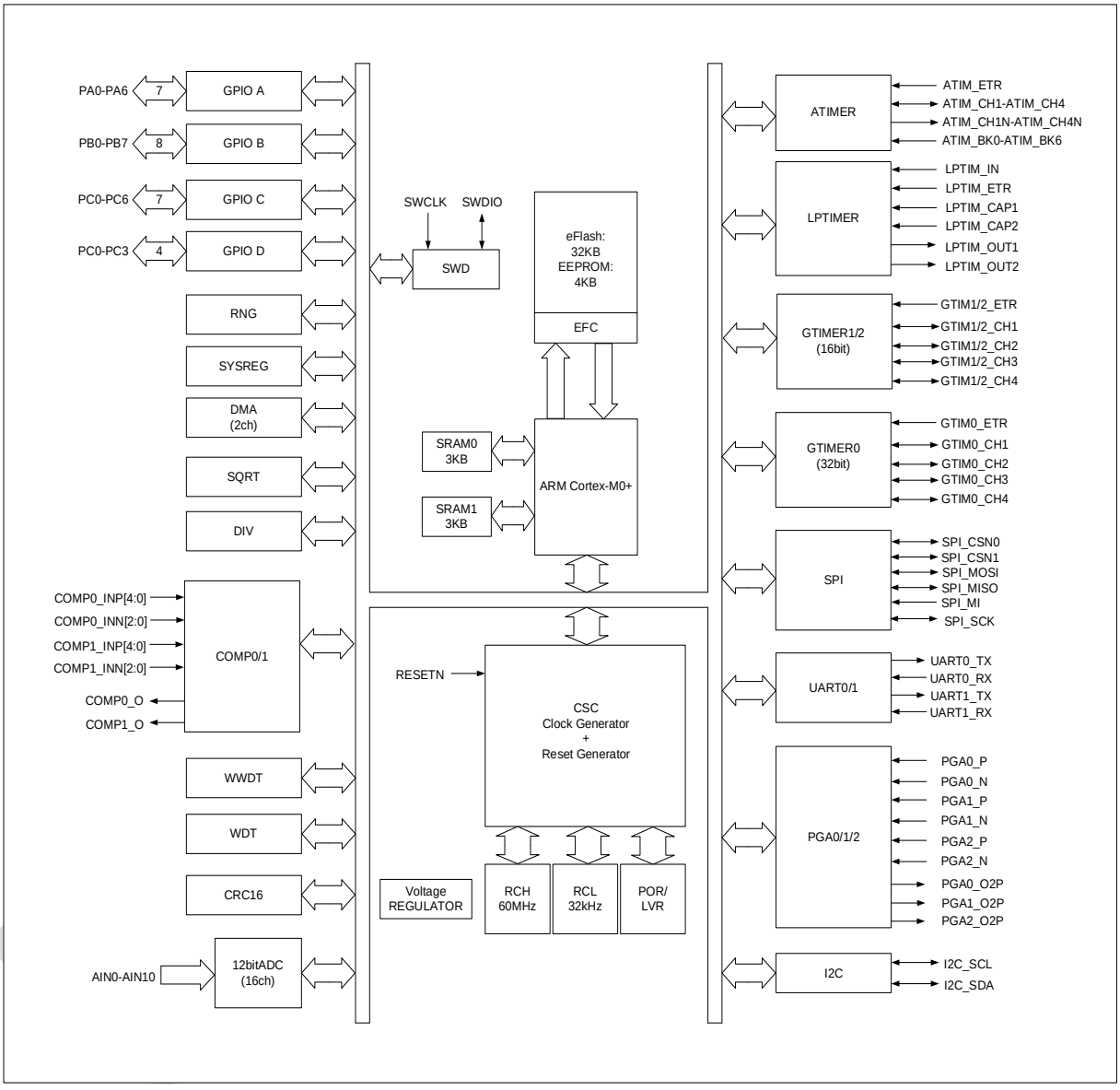


Figure 3-4: UM32M156-G6P7 Block Diagram

3.2.2 UM32MP56-E6P7

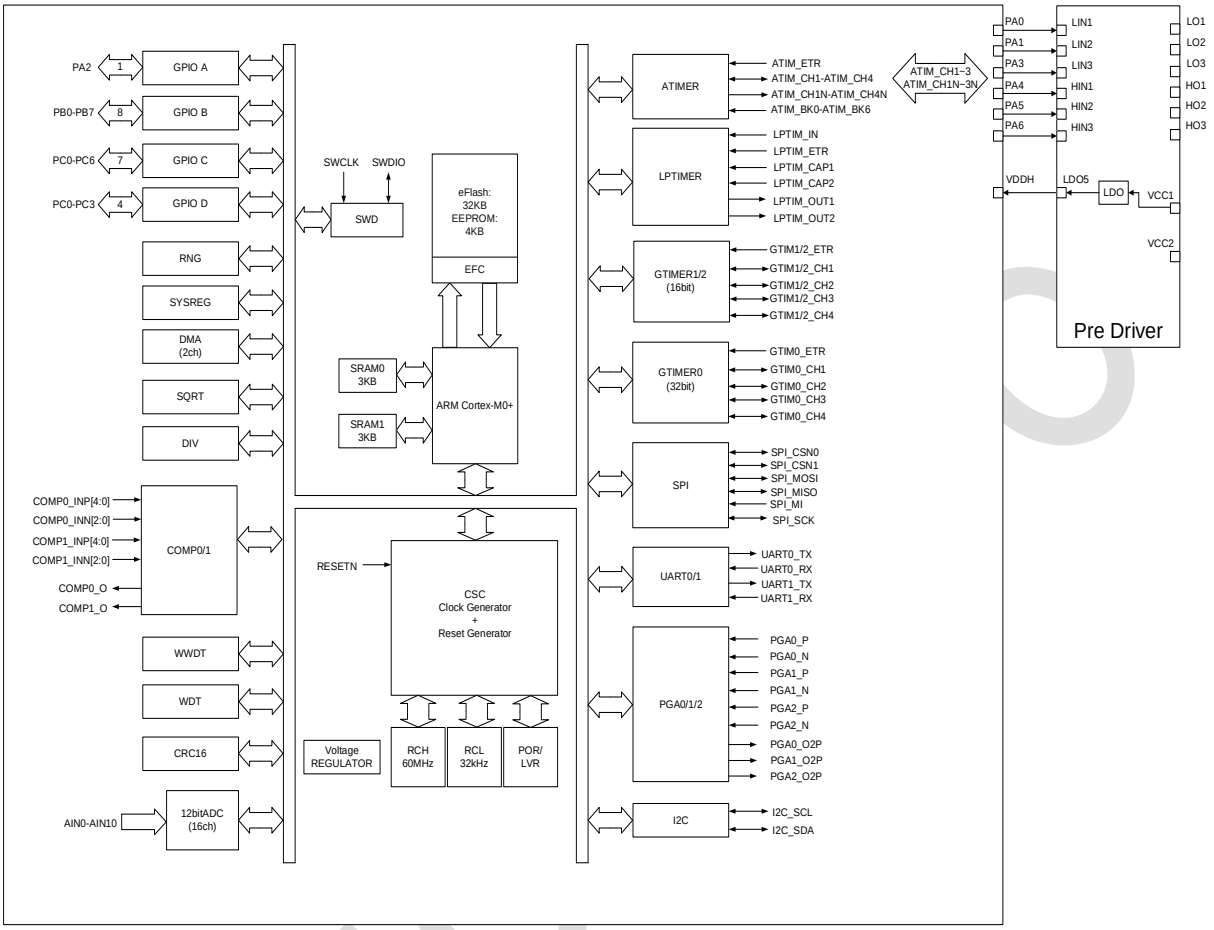


Figure 3-5: UM32MP56-E6P7 Block Diagram

3.2.3 UM32MP56-H6U7

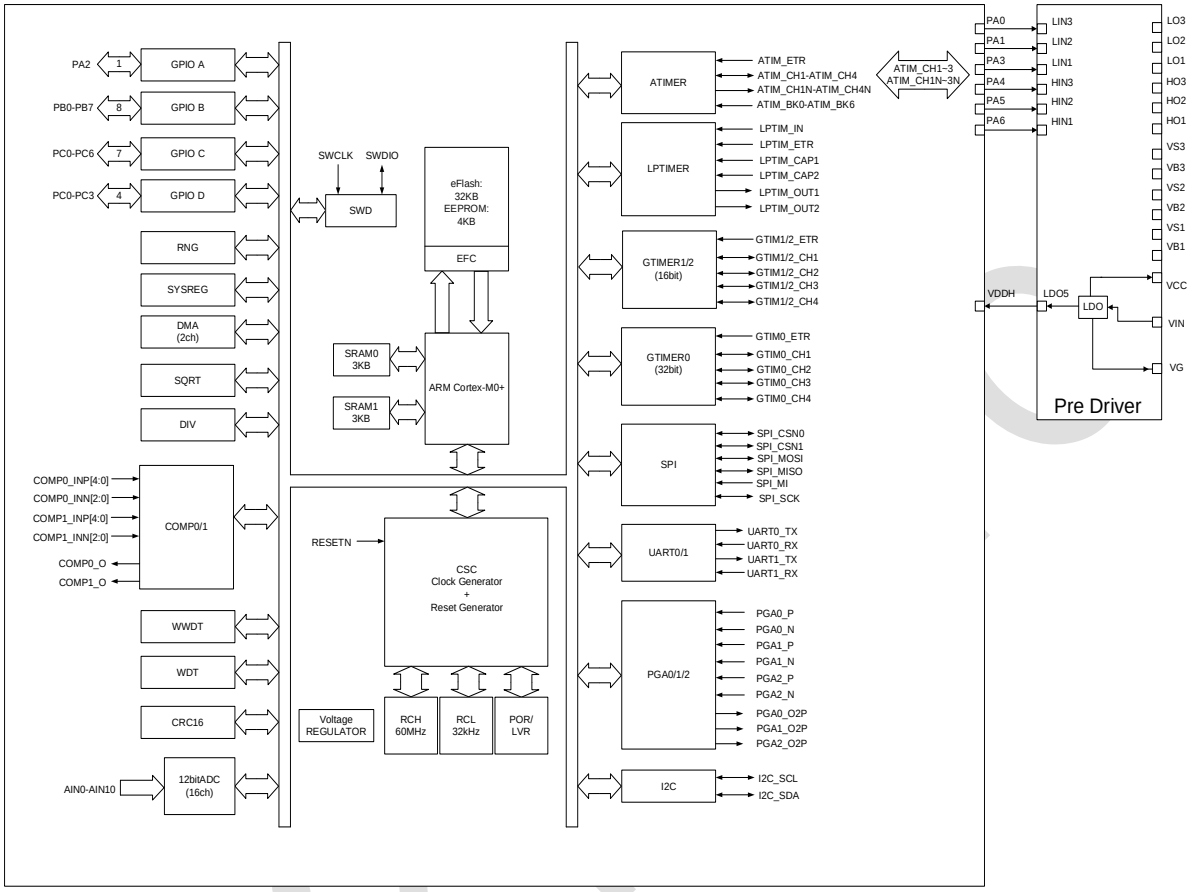


Figure 3-6: UM32MP56-H6U7 Block Diagram

3.3 Internal Analog Signal Connection of the Product

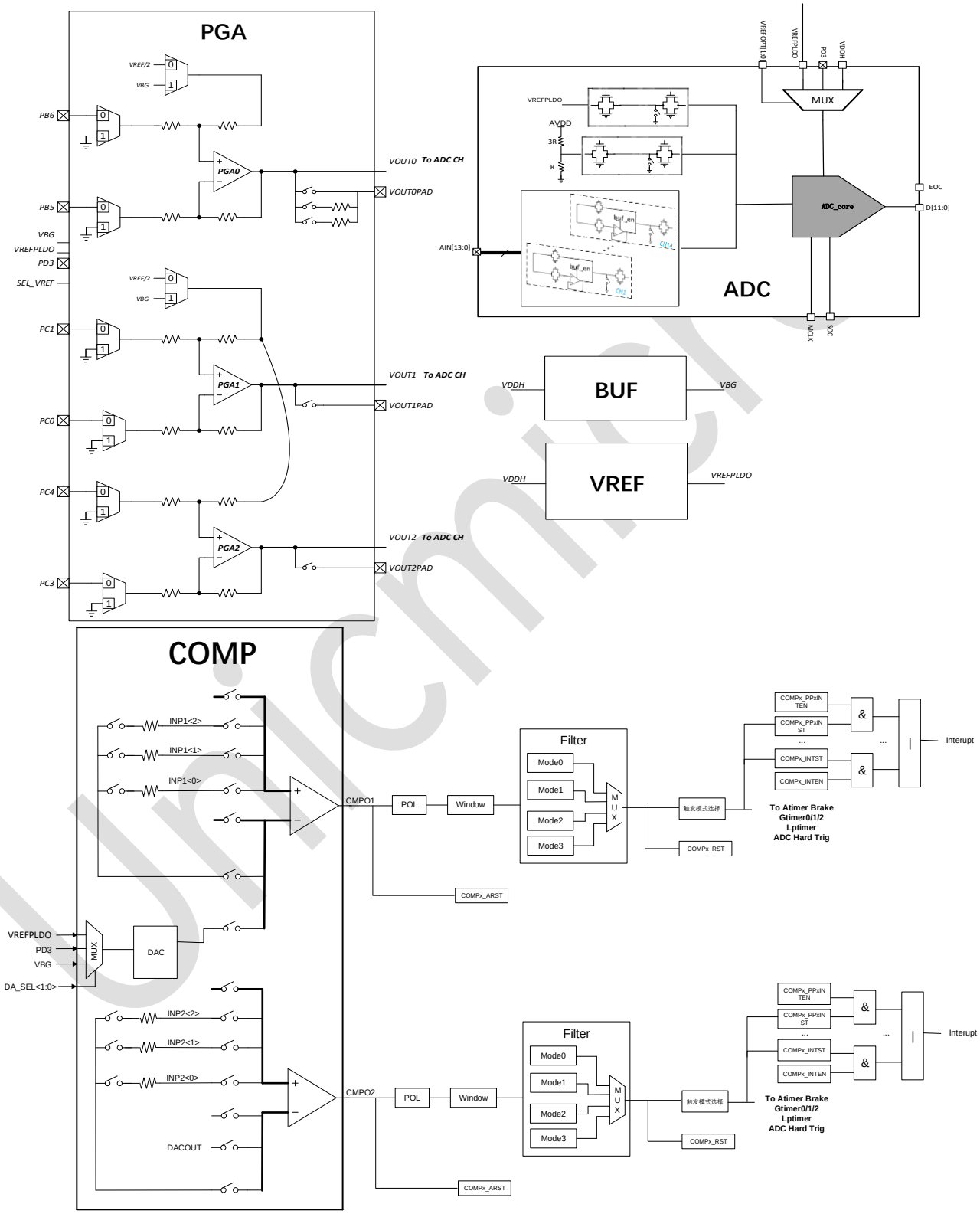


Figure 3-7: Internal Analog Signal Connection of the Product

The BUF output is a VBG signal, which can be set as the reference voltage for the DAC inside the comparator or as the reference voltage for the PGA. The output of the PGA can be configured as the sampling channel of the ADC and can also be set as the P terminal of COMP0/1. The comparator contains a built-in 7-bit DAC, which can be used as the N terminal of the comparator. The output of VREF can be set as the sampling channel of the ADC.

3.4 Alternate Function

Table 3-1: Pin Alternate Function

			Config	Px_SEL[i+2;i]															
TSSOP28	SSOP24	QFN40		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1	-	-	-	PA0	UART0_TX	GTIM0_CH1	GTIM1_CH2	GTIM1_ETR	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	-	-	-	-
2	-	-	-	PA1	UART0_RX	GTIM0_CH2	GTIM1_CH3	GTIM2_ETR	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	-	-	-	-
3	-	-	-	PA3	UART1_TX	GTIM0_CH3	GTIM1_CH4	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	LVD_OUT	-	-	-	-
4	-	-	-	PA4	UART1_RX	GTIM1_CH2	SPI_MISO	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	LPTIM_CAP2	-	-	-	-
5	-	-	-	PA5	GTIM1_CH2	GTIM2_CH2	SPI_CSN0	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	ATIM_BK0	-	-	-	-
6	-	-	-	PA6	GTIM1_CH1	GTIM1_ETR	GTIM2_CH1	SPI_SCK	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	-	-	-	-
7	-	31	COMP1_INP2/ AIN10	PB0	UART0_RX	GTIM0_CH1	GTIM0_ETR	GTIM1_CH2	GTIM1_ETR	GTIM2_CH3	SPI_CSN0	SPI_MOSI	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3N	I2C_SCL	-
8	-	32	COMP0_INN2/ COMP1_INP1/ AIN9	PB1	UART0_TX	GTIM0_CH2	GTIM0_ETR	GTIM1_CH3	GTIM2_CH2	SPI_CSN1	SPI_SCK	SPI_MOSI	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	CLK_OUT	I2C_SDA	-	-
9	20	33	COMP1_INP0/ AIN8	PB2	GTIM0_CH1	GTIM0_CH3	GTIM0_ETR	GTIM2_CH1	GTIM2_CH4	SPI_MISO	SPI_MI1	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_BK1	I2C_SCL	-	-
10	16	40	COMP0_INP3/ COMP1_INP3/ PGA0_O2P/ AIN6	PB4	UART1_TX	GTIM0_CH3	GTIM0_ETR	GTIM1_CH2	GTIM1_ETR	GTIM2_CH3	GTIM2_ETR	SPI_CSN0	SPI_MISO	SPI_MOSI	ATIM_CH4	I2C_SDA	-	-	-
11	17	39	COMP0_INN1/ COMP1_INN1/ PGA0_N	PB5	UART1_RX	GTIM0_CH2	GTIM1_CH1	GTIM1_CH4	GTIM2_CH2	GTIM2_CH3	SPI_CSN1	SPI_MISO	SPI_MOSI	CLK_OUT	LPTIM_OUT2	COMP1_OUT	-	-	-

			Config	Px_SEL[i+2;i]															
TSSOP28	SSOP24	QFN40		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
12	18	38	COMP0_INP2/ PGA0_P	PB6	GTIM0_CH1	GTIM0_CH4	GTIM1_CH3	GTIM2_CH1	GTIM2_CH2	SPI_SCK	ATIM_ETR	LPTIM_OUT1	LPTIM_IN	LPTIM_CAP2	COMP0_OUT	-	-	-	-
13	20	36	COMP0_INN0/ COMP1_INN0/ PGA1_N	PC0	UART1_RX	GTIM0_CH2	GTIM1_CH1	GTIM2_CH2	GTIM2_CH3	SPI_CSN1	SPI_MISO	SPI_MI1	LPTIM_OUT1	LPTIM_CAP1	I2C_SDA	-	-	-	-
14	19	35	COMP0_INP0/ PGA1_P	PC1	UART1_TX	GTIM0_CH1	GTIM0_CH4	GTIM1_CH4	GTIM2_CH2	GTIM2_ETR	SPI_SCK	LVD_OUT	LPTIM_OUT2	LPTIM_IN	LPTIM_CAP2	-	-	-	-
15	-	37	COMP0_INP1/ COMP1_INP4/ PGA1_O2P/ AIN5	PB7	UART1_RX	GTIM0_CH2	GTIM0_CH3	GTIM0_ETR	GTIM1_CH2	GTIM1_CH3	GTIM1_ETR	GTIM2_CH3	GTIM2_ETR	SPI_CSN0	SPI_MOSI	ATIM_ETR	ATIM_BK4	LPTIM_ETR	I2C_SCL
16	-	34	COMP1_INN2/ AIN7	PB3	UART0_TX	UART0_RX	GTIM0_CH4	GTIM1_CH1	GTIM1_CH3	GTIM2_CH1	SPI_CSN1	SPI_SCK	SPI_MOSI	ATIM_CH1	ATIM_CH1N	-	-	-	-
17	21	1	COMP0_INP4/ PGA2_O2P/ AIN0	PC2	UART0_RX	GTIM0_CH1	GTIM0_CH3	GTIM0_ETR	GTIM1_CH2	GTIM1_CH3	GTIM1_ETR	GTIM2_CH4	ATIM_ETR	ATIM_BK6	ADC_TRO	COMP1_OUT	-	-	-
18	21	2	PGA2_N	PC3	UART0_TX	GTIM0_CH2	GTIM0_ETR	GTIM1_CH1	GTIM1_CH3	GTIM1_CH4	GTIM2_CH1	GTIM2_CH3	ATIM_CH1N	ATIM_ETR	ADC_TRO	LPTIM_IN	LPTIM_CAP2	CAMP0_OUT	-
19	22	3	PGA2_P	PC4	UART0_RX	GTIM0_CH1	GTIM1_CH2	GTIM1_CH3	GTIM2_CH3	GTIM2_ETR	SPI_MOSI	ATIM_CH2N	ATIM_CH3	ATIM_ETR	ATIM_BK5	ADC_TRO	I2C_SDA	COMP1_OUT	-
20	23	4	AIN1	PD0	UART0_TX	GTIM0_CH2	GTIM0_CH3	GTIM0_ETR	GTIM1_CH1	SPI_CSN0	SPI_CSN1	SPI_SCK	ATIM_CH2N	ATIM_CH3	ATIM_ETR	ATIM_BK3	ADC_TRO	I2C_SCL	COMP1_OUT
21	24	5	AIN2	PD1	UART0_TX	UART1_RX	GTIM0_CH1	GTIM0_ETR	GTIM1_ETR	GTIM2_CH2	SPI_MISO	SPI_MI1	ATIM_CH3	ATIM_CH3N	ATIM_ETR	ADC_TRO	I2C_SDA	COMP0_OUT	-
22	1	6	AIN3	PD2	UART1_TX	GTIM0_CH3	GTIM0_ETR	GTIM2_CH1	GTIM2_CH2	GTIM2_CH3	SPI_SCK	SPI_MOSI	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	I2C_SCL
23	2	7	AIN4	PD3	UART1_RX	GTIM0_CH2	GTIM2_CH1	SPI_MOSI	ATIM_CH1	ATIM_CH1N	ATIM_CH2	ATIM_CH2N	ATIM_CH3	ATIM_CH3N	ATIM_CH4	ATIM_ETR	ATIM_BK2	ADC_TRO	I2C_SDA

			Config	Px_SEL[i+2;i]															
TSSOP28	SSOP24	QFN40		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
24	3	8	RESETN	PA2	-	GTIM0_CH1	GTIM1_CH2	GTIM2_CH1	GTIM2_CH3	SPI_MOSI	ATIM_ETR	LPTIM_ETR	LPTIM_CAP1	I2C_SCL	I2C_SDA	-	-	-	-
25	4	9	-	PC5	SWIO	UART0_RX	UART1_TX	GTIM1_CH1	GTIM2_CH2	GTIM2_CH3	SPI_SCK	SPI_MI1	CLK_OUT	I2C_SCL	COMP0_OUT	-	-	-	-
26	5	10	-	PC6	SWCLK	UART0_TX	GTIM1_CH3	GTIM2_CH1	GTIM2_CH4	SPI_CSN0	SPI_MISO	SPI_MOSI	ATIM_ETR	I2C_SDA	COMP1_OUT	-	-	-	-
27	6	14	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
28	7	13	VDDH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	11/ 12/ 27	NC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	7	13	LDO5	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	8	-	VCC1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	9	-	VCC2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	10	25	HO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	11	17	LO1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	12	22	HO2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	13	16	LO2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	14	19	HO3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	15	15	LO3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	18	VS3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	20	VB3	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	21	VS2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	23	VB2	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	24	VS1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	26	VB1	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	28	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	29	VG	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	30	VIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-

3.5 Pin Description

Table 3-2: Pin Definition

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
1	-	-	PA0	I/O	HZ	HZ	PA0	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							GTIM0_CH1	Input capture/PWM output channel 1 of GTIMER0
							GTIM1_CH2	Input capture/PWM output channel 2 of GTIMER1
							GTIM1_ETR	Input ETR signal of GTIMER1
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
2	-	-	PA1	I/O	HZ	HZ	PA1	General-purpose digital input/output pin

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							UART0_RX	RX signal of UART0
							GTIM0_CH2	Input capture/PWM output channel 2 of GTIMER0
							GTIM1_CH3	Input capture/PWM output channel 3 of GTIMER1
							GTIM2_ETR	Input ETR signal of GTIMER2
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
3	-	-	PA3	I/O	DI	HZ	PA3	General-purpose digital input/output pin
							UART1_TX	TX signal of UART1
							GTIM0_CH3	Input capture/PWM output channel 3 of GTIMER0
							GTIM1_CH4	Input capture/PWM output channel 4 of GTIMER1
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
							LVD_OUT	LVD output signal
4	-	-	PA4	I/O	DI	HZ	PA4	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							GTIM1_CH2	Input capture/PWM output channel 2 of GTIMER1
							SPI_MISO	MISO signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
							LPTIM_CAP2	Input capture signal of channel 2 of LPTIMER
5	-	-	PA5	I/O	HZ	HZ	PA5	General-purpose digital input/output pin
							GTIM1_CH2	Input capture/PWM output channel 2 of GTIMER1
							GTIM2_CH2	Input capture/PWM output channel 2 of GTIMER2
							SPI_CSN0	CSN0 signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
							ATIM_BK0	Break input signal 0 of ATIMER
6	-	-	PA6	I/O	HZ	HZ	PA6	General-purpose digital input/output pin
							GTIM1_CH1	Input capture / PWM output signal of GTIMER1
							GTIM1_ETR	Input ETR signal of GTIMER1
							GTIM2_CH1	Input capture / PWM output signal of GTIMER2
							SPI_SCK	SCK signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
7	-	31	PB0	I/O	HZ	HZ	PB0	General-purpose digital input/output pin
							UART0_RX	RX signal of UART0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_CH2	Input capture/PWM output signal 2 of GTIMER1
							GTIM1_ETR	Input ETR signal of GTIMER1
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							SPI_CSN0	SPI CSN0 signal
							SPI_MOSI	MOSI signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							I2C_SCL	I2C clock
							COMP1_INP2	INP1 input signal of comparator 1
							AIN10	ADC channel 10
8	-	32	PB1	I/O	HZ	HZ	PB1	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							SPI_CSN1	SPI CSN1 signal
							SPI_SCK	SCK signal of SPI
							SPI_MOSI	MOSI signal of SPI
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							CLK_OUT	Clock output pin
							I2C_SDA	I2C data
							COMP0_INP2	INP2 input signal of comparator 0
							COMP1_INP1	INP1 input signal of comparator 1
							AIN9	ADC channel 9
9	20	33	PB2	I/O	HZ	HZ	PB2	General-purpose digital input/output pin
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM0_CH3	Input capture/PWM output signal 3 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM2_CH4	Input capture/PWM output signal 4 of GTIMER2
							SPI_MISO	MISO signal of SPI
							SPI_MI	MISO signal of SPI, master mode only
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_BK1	Break input signal 1 of ATIMER
							I2C_SCL	I2C clock
							COMP1_INP0	INP0 input signal of comparator 1
							AIN8	ADC channel 8
10	16	40	PB4	I/O	HZ	HZ	PB4	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							GTIM0_CH3	Input capture/PWM output signal 3 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_CH2	Input capture/PWM output signal 2 of GTIMER1
							GTIM1_ETR	Input ETR signal of GTIMER1
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM2_ETR	Input ETR signal of GTIMER2
							SPI_CSN0	SPI CSN0 signal
							SPI_MISO	MISO signal of SPI
							SPI_MOSI	MOSI signal of SPI
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
							I2C_SDA	I2C data
							COMP0_INP3	INP3 input signal of comparator 0
							COMP1_INP3	INP3 input signal of comparator 1
							PGA0_O2P	O2P of PGA0
							AIN6	ADC channel 6
11	17	39	PB5	I/O	HZ	HZ	PB5	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0
							GTIM1_CH1	Input capture/PWM output signal 1 of GTIMER1
							GTIM1_CH4	Input capture/PWM output signal 4 of GTIMER1
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							SPI_CSN1	SPI CSN1 signal
							SPI_MISO	MISO signal of SPI
							SPI_MOSI	MOSI signal of SPI
							CLK_OUT	Clock output pin
							LPTIM_OUT2	PWM output signal of channel 2 of LPTIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							COMP1_OUT	Output signal of comparator 1
							COMP0_INN1	INN1 input signal of comparator 0
							COMP1_INN1	INN1 input signal of comparator 1
							PGA0_N	N terminal of PGA0
12	18	38	PB6	I/O	HZ	HZ	PB6	General-purpose digital input/output pin
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM0_CH4	Input capture/PWM output signal 4 of GTIMER0
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							SPI_SCK	SCK signal of SPI
							ATIM_ETR	ETR signal of ATIMER
							LPTIM_OUT1	PWM output signal of channel 1 of LPTIMER
							LPTIM_IN	External clock input signal of LPTIMER
							LPTIM_CAP2	Input capture signal of channel 2 of LPTIMER
							COMP0_OUT	Output signal of comparator 0
							COMP0_INP2	INP2 input signal of comparator 0
							PGA0_P	P terminal of PGA0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
13	20	36	PC0	I/O	HZ	HZ	PC0	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0
							GTIM1_CH1	Input capture/PWM output signal 1 of GTIMER1
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							SPI_CSN1	SPI CSN1 signal
							SPI_MISO	MISO signal of SPI
							SPI_MI	MISO signal of SPI, master mode only
							LPTIM_OUT1	PWM output signal of channel 1 of LPTIMER
							LPTIM_CAP1	Input capture signal of channel 1 of LPTIMER
							I2C_SDA	I2C data
							COMP0_INN0	INN0 input signal of comparator 0
							COMP1_INN0	INN0 input signal of comparator 1
							PGA1_P	P terminal of PGA1
14	19	35	PC1	I/O	HZ	HZ	PC1	General-purpose digital input/output pin
							UART1_TX	TX signal of UART1
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM0_CH4	Input capture/PWM output signal 4 of GTIMER0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM1_CH4	Input capture/PWM output signal 4 of GTIMER1
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							GTIM2_ETR	Input ETR signal of GTIMER2
							SPI_SCK	SCK signal of SPI
							LVD_OUT	LVD output signal
							LPTIM_OUT2	PWM output signal of channel 2 of LPTIMER
							LPTIM_IN	External clock input signal of LPTIMER
							LPTIM_CAP2	Input capture signal of channel 2 of LPTIMER
							COMP0_INP0	INP0 input signal of comparator 0
							PGA1_P	P terminal of PGA1
15	-	37	PB7	I/O	HZ	HZ	PB7	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0
							GTIM0_CH3	Input capture/PWM output signal 3 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_CH2	Input capture/PWM output signal 2 of GTIMER1
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM1_ETR	Input ETR signal of GTIMER1
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							GTIM2_ETR	Input ETR signal of GTIMER2

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							SPI_CSN0	SPI CSN0 signal
							SPI_MOSI	MOSI signal of SPI
							ATIM_ETR	ETR signal of ATIMER
							ATIM_BK4	Break input signal 4 of ATIMER
							LPTIM_ETR	ETR signal of LPTIMER
							I2C_SCL	I2C clock
							COMP0_INP1	INP1 input signal of comparator 0
							COMP1_INP4	INP4 input signal of comparator 1
							PGA1_O2P	O2P of PGA1
							AIN5	ADC channel 5
16	-	34	PB3	I/O	HZ	HZ	PB3	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							UART0_RX	RX signal of UART0
							GTIM0_CH4	Input capture/PWM output signal 4 of GTIMER0
							GTIM1_CH1	Input capture/PWM output signal 1 of GTIMER1
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2
							SPI_CSN1	SPI CSN1 signal
							SPI_SCK	SCK signal of SPI
							SPI_MOSI	MOSI signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							COMP1_INN2	INN2 input signal of comparator 1
							AIN7	ADC channel 7
17	21	1	PC2	I/O	HZ	HZ	PC2	General-purpose digital input/output pin
							UART0_RX	RX signal of UART0
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM0_CH3	Input capture/PWM output signal 3 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_CH2	Input capture/PWM output signal 2 of GTIMER1
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM1_ETR	Input ETR signal of GTIMER1
							GTIM2_CH4	Input capture/PWM output signal 4 of GTIMER2
							ATIM_ETR	ETR signal of ATIMER
							ATIM_BK6	Break input signal 6 of ATIMER
							ADC_TRO	TRO signal of ADC
							COMP1_OUT	Output signal of comparator 1
							COMP0_INP4	INP4 input signal of comparator 0
							PGA2_O2P	O2P of PGA2
							AIN0	ADC channel 0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
18	21	2	PC3	I/O	HZ	HZ	PC3	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_CH1	Input capture/PWM output signal 1 of GTIMER1
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM1_CH4	Input capture/PWM output signal 4 of GTIMER1
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_ETR	ETR signal of ATIMER
							ADC_TRO	TRO signal of ADC
							LPTIM_IN	External clock input signal of LPTIMER
							LPTIM_CAP2	Input capture signal of channel 2 of LPTIMER
							COMP0_OUT	Output signal of comparator 0
							PGA2_N	N terminal of PGA2
19	22	3	PC4	I/O	HZ	HZ	PC4	General-purpose digital input/output pin
							UART0_RX	RX signal of UART0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM1_CH2	Input capture/PWM output signal 2 of GTIMER1
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							GTIM2_ETR	Input ETR signal of GTIMER2
							SPI_MOSI	MOSI / DC signal of SPI0
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_ETR	ETR signal of ATIMER
							ATIM_BK5	Break input signal 5 of ATIMER
							ADC_TRO	TRO signal of ADC
							I2C_SDA	I2C data
							COMP1_OUT	Output signal of comparator 1
							PGA2_P	P terminal of PGA2
20	23	4	PD0	I/O	HZ	HZ	PD0	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0
							GTIM0_CH3	Input capture/PWM output signal 3 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							GTIM1_CH1	Input capture/PWM output signal 1 of GTIMER1
							SPI_CSN0	SPI CSN0 signal
							SPI_CSN1	SPI CSN1 signal
							SPI_SCK	SCK signal of SPI
							ATIM_CH2N	Complementary channel of PWM output channel 2 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_ETR	ETR signal of ATIMER
							ATIM_BK3	Break input signal 3 of ATIMER
							ADC_TRO	TRO signal of ADC
							I2C_SCL	I2C clock
							COMP1_OUT	Output signal of comparator 1
							AIN1	ADC channel 1
21	24	5	PD1	I/O	HZ	HZ	PD1	General-purpose digital input/output pin
							UART0_TX	TX signal of UART0
							UART1_RX	RX signal of UART1
							GTIM0_CH1	Input capture/PWM output signal 1 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM1_ETR	Input ETR signal of GTIMER1
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							SPI_MISO	MISO signal of SPI
							SPI_MI	MISO signal of SPI, master mode only

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_ETR	ETR signal of ATIMER
							ADC_TRO	TRO signal of ADC
							I2C_SDA	I2C data
							COMP0_OUT	Output signal of comparator 0
							AIN2	ADC channel 2
22	1	6	PD2	I/O	HZ	HZ	PD2	General-purpose digital input/output pin
							UART1_TX	TX signal of UART1
							GTIM0_CH3	Input capture/PWM output signal 3 of GTIMER0
							GTIM0_ETR	Input ETR signal of GTIMER0
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							SPI_SCK	SCK signal of SPI
							SPI_MOSI	MOSI signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH2N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							I2C_SCL	I2C clock
							AIN3	ADC channel 3
23	2	7	PD3	I/O	HZ	HZ	PD3	General-purpose digital input/output pin
							UART1_RX	RX signal of UART1
							GTIM0_CH2	Input capture/PWM output signal 2 of GTIMER0
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2
							SPI_MOSI	MOSI signal of SPI
							ATIM_CH1	Input capture/PWM output channel 1 of ATIMER
							ATIM_CH1N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH2	Input capture/PWM output channel 2 of ATIMER
							ATIM_CH2N	Complementary channel of PWM output channel 1 of ATIMER
							ATIM_CH3	Input capture/PWM output channel 3 of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							ATIM_CH3N	Complementary channel of PWM output channel 3 of ATIMER
							ATIM_CH4	Input capture/PWM output channel 4 of ATIMER
							ATIM_ETR	ETR signal of ATIMER
							ATIM_BK2	Break input signal 2 of ATIMER
							ADC_TRO	TRO signal of ADC
							I2C_SDA	I2C data
							AIN4	ADC channel 4
24	3	8	RESETN	I/O	DI	PU	PA2	General-purpose digital input/output pin
							RESETN (default)	External reset input
							GTIM0_CH1	Input capture/PWM output channel 1 of GTIMER0
							GTIM1_CH2	Input capture/PWM output channel 2 of GTIMER1
							GTIM2_CH1	Input capture/PWM output channel 1 of GTIMER2
							GTIM2_CH3	Input capture/PWM output channel 3 of GTIMER2
							SPI0_MOSI	MOSI / DC signal of SPI0
							ATIM_ETR	ETR signal of ATIMER
							LPTIM_ETR	ETR signal of LPTIMER0
							LPTIM_CAP1	Input capture signal of channel 1 of LPTIMER
							I2C_SCL	I2C clock
							I2C_SDA	I2C data
25	4	9	PC5	I/O	DI	PU	PC5	General-purpose digital input/output pin

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							SWIO (default)	Data signal of JTAG SWD
							UART0_RX	RX signal of UART0
							UART1_TX	TX signal of UART1
							GTIM1_CH1	Input capture/PWM output signal 1 of GTIMER1
							GTIM2_CH2	Input capture/PWM output signal 2 of GTIMER2
							GTIM2_CH3	Input capture/PWM output signal 3 of GTIMER2
							SPI_SCK	SCK signal of SPI
							SPI_MI	MISO signal of SPI, master mode only
							CLK_OUT	Clock output pin
							I2C_SCL	I2C clock
							COMP0_OUT	Output signal of comparator 0
26	5	10	PC6	I/O	DI	PD	PC6	General-purpose digital input/output pin
							SWCLK (default)	Clock signal of JTAG SWD
							UART0_TX	TX signal of UART0
							GTIM1_CH3	Input capture/PWM output signal 3 of GTIMER1
							GTIM2_CH1	Input capture/PWM output signal 1 of GTIMER2
							GTIM2_CH4	Input capture/PWM output signal 4 of GTIMER2
							SPI_CSN0	SPI CSN0 signal
							SPI_MISO	MISO signal of SPI
							SPI_MOSI	MOSI signal of SPI
							ATIM_ETR	ETR signal of ATIMER

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
							I2C_SDA	I2C data
							COMP1_OUT	Output signal of comparator 1
27	–	–	VSS	G	–	–	VSS	Connect to PCB ground
28	–	–	VDDH	P	–	–	VDDH	External power input to the chip
–	7	13	LDO5	O	–	–	LDO5	5 V output terminal
–	8	–	VCC1	P	–	–	VCC1	5 V power supply terminal
–	9	–	VCC2	P	–	–	VCC2	Drive power supply terminal
–	10	25	HO1	O	–	–	HO1	High-side output signal of phase 1
–	11	17	LO1	O	–	–	LO1	Low-side output signal of phase 1
–	12	22	HO2	O	–	–	HO2	High-side output signal of phase 2
–	13	16	LO2	O	–	–	LO2	Low-side output signal of phase 2
–	14	19	HO3	O	–	–	HO3	High-side output signal of phase 3
–	15	15	LO3	O	–	–	LO3	Low-side output signal of phase 3
–	–	18	VS3	P	–	–	VS3	High-side floating ground of phase 3
–	–	20	VB3	P	–	–	VB3	High-side floating source of phase 3
–	–	21	VS2	P	–	–	VS2	High-side floating ground of phase 2
–	–	23	VB2	P	–	–	VB2	High-side floating source of phase 2
–	–	24	VS1	P	–	–	VS1	High-side floating ground of phase 1

Pin No. in Each Package			Pin Name	IO Type	Reset Status		Pin Type	Functional Description
TSSOP28	SSOP24	QFN40			DIR	PU PD		
–	–	26	VB1	P	–	–	VB1	High-side floating source of phase 1
–	–	28	VCC	P	–	–	VCC	Supply voltage
–	–	29	VG	O	–	–	VG	External MOSFET gate drive
–	–	30	VIN	P	–	–	VIN	Analog power

Note: A—analog signal; D—digital signal; I—input; O—output; G—ground; P—power; PU—pull up; PD—pull down; HZ—high impedance state.

3.6 SIP Inline Signal Description

3.6.1 UM32MP56-E6P7

Table 3-3: SIP Inline Signal Description

Pin	Pin Description
HO1	HO1, the high-side output signal of phase 1, controlled by MCU PA4 output signal, is in phase with PA4 signal, that is, when the input is “1”, HO1 outputs “1”.
LO1	LO1, the low-side output signal of phase 1, controlled by MCU PA0 output signal, is in phase with PA0 signal, that is, when the input is “0”, LO1 outputs “1”.
HO2	HO2, the high-side output signal of phase 2, controlled by MCU PA5 output signal, is in phase with PA5 signal, that is, when the input is “1”, HO2 outputs “1”.
LO2	LO2, the low-side output signal of phase 2, controlled by MCU PA1 output signal, is in phase with PA1 signal, that is, when the input is “0”, LO2 outputs “0”.
HO3	HO3, the high-side output signal of phase 3, controlled by MCU PA6 output signal, is in phase with PA6 signal, that is, when the input is “1”, HO3 outputs “1”.
LO3	LO3, the low-side output signal of phase 3, controlled by MCU PA3 output signal, is in phase with PA3 signal, that is, when the input is “0”, LO3 outputs “0”.

3.6.2 UM32MP56-H6U7

Table 3-4: SIP Inline Signal Description

Pin	Pin Description
LO3	LO3, the low-side output signal of phase 3, controlled by MCU PA0 output signal, is in phase with PA0 signal, that is, when the input is “0”, LO3 outputs “0”.
LO2	LO2, the low-side output signal of phase 2, controlled by MCU PA1 output signal, is in phase with PA1 signal, that is, when the input is “0”, LO2 outputs “0”.
LO1	LO1, the low-side output signal of phase 1, controlled by MCU PA3 output signal, is in phase with PA3 signal, that is, when the input is “0”, LO1 outputs “1”.
HO3	HO3, the high-side output signal of phase 3, controlled by MCU PA4 output signal, is in phase with PA4 signal, that is, when the input is “1”, HO3 outputs “1”.
HO2	HO2, the high-side output signal of phase 2, controlled by MCU PA5 output signal, is in phase with PA5 signal, that is, when the input is “1”, HO2 outputs “1”.
HO1	HO1, the high-side output signal of phase 1, controlled by MCU PA6 output signal, is in phase with PA6 signal, that is, when the input is “1”, HO1 outputs “1”.

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{ss}.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all products are tested on the production line at T_A = 25℃. The maximum and minimum values support the worst-case environmental temperature, supply voltage, and clock frequency as specified.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3Σ).

4.1.2 Typical Value

Unless otherwise specified, typical data are measured based on T_A = 25 ℃ and V_{DDH} = 3.3 V. They are given only as design guidelines.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Power Supply Scheme

The chip supports single power supply and VBAT backup power supply. It requires an external operating supply voltage between 2.3 V and 5.5 V, and a digital circuit operating voltage generated by the built-in LDO.

The system power supply scheme is shown below.

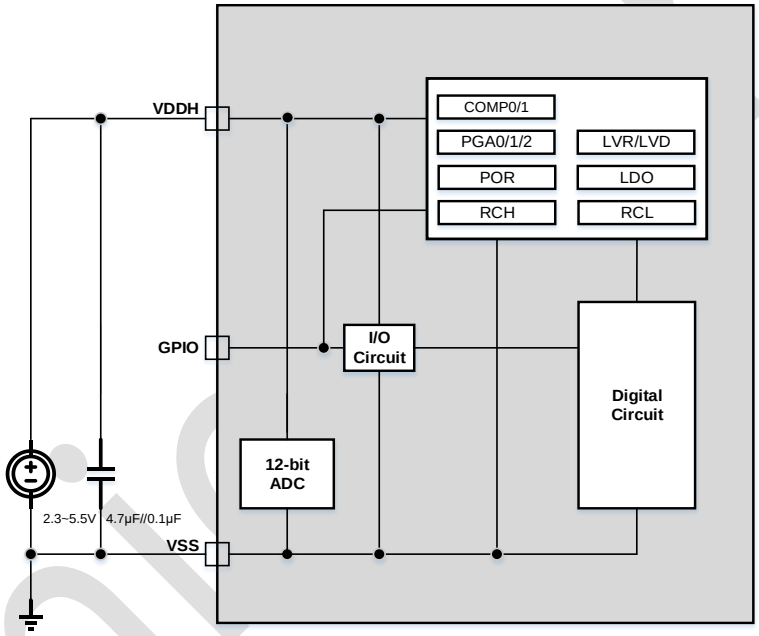


Figure 4-1: Block Diagram of Power Supply Scheme

4.2 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 4-1, Table 4-2 and Table 4-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
V_{DDH} – V_{SS}	External main supply voltage(1)	-0.3	5.8	V
V_{IN}	Input voltage on the pin(2)	V_{SS} – 0.3	V_{DDH} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	–	50	mV
$\|V_{SSX} - V_{SS}\|$	Voltage difference between different ground pins	–	50	

Notes:

1. All main power (V_{DDH}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

Table 4-2: Current Characteristics

Symbol	Description	Max. (1)	Unit
I_{VDDH}	Total current through the V_{DDH-} power line (supply current)(1) (3)	200	mA
I_{VSS}	Total current through the V_{SS} ground line (output current)(1) (3)	200	
$I_{INJ(PIN)}$(2)	Injection current on NRST pin	-5	
	Injection current on other pins	±5	

Notes:

1. All main power (V_{DDH}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.
2. A positive injection is induced by $V_{IN} > V_{DDH}$, and a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ maximum must always be respected. Refer to Table 4-1for the maximum allowed injected current values.
3. When the maximum current occurs, the maximum voltage drop of V_{DDH} is allowed to be $0.1V_{DDH}$.

Table 4-3: Thermal Characteristics

Symbol	Description	Value	Unit
T_{stg}	Storage temperature range	-55–+150	℃
T_J	Maximum junction temperature	110	℃

4.3 Operating Condition

Static parameter table (applicable temperature range: T_A = -40℃ – +105℃).

4.3.1 General Operating Condition

Table 4-4: General Operating Condition

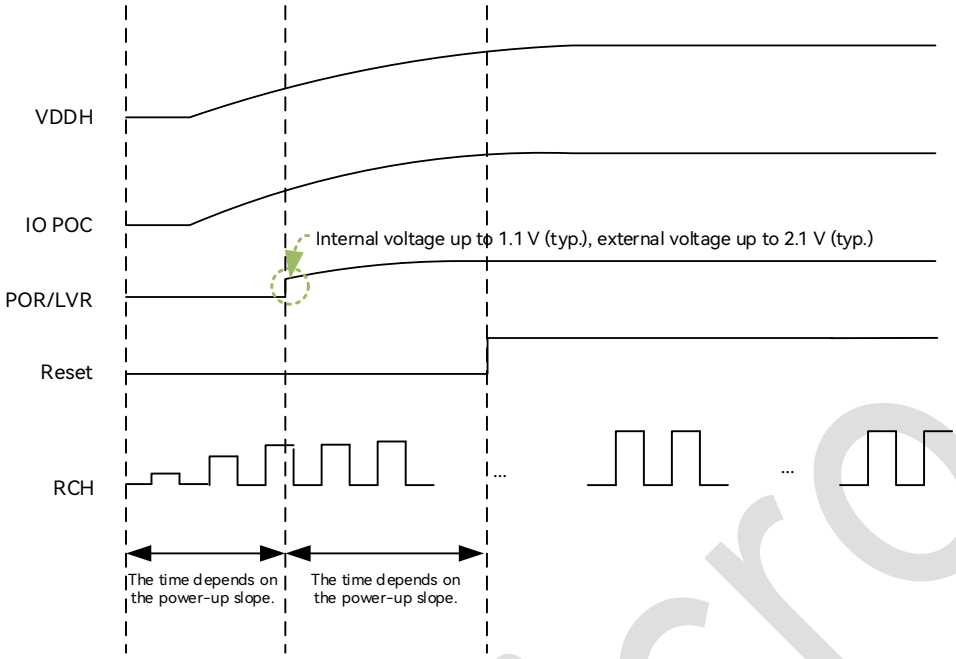
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	60	60	MHz
f_{PCLK}	Internal APB clock frequency	-	0	60	60	
V_{DDH}	Standard operating voltage	-	2.3	-	5.5	V
T_A	Ambient temperature	-	-40	-	105	℃
f_{sys}	System frequency	-	0.1	-	60	MHz
T_J	Junction temperature range	-	-40	-	110	℃

*: When f_{sys} is lower than 7.5 MHz, Flash can only fetch and execute code, but cannot erase or write.

4.3.2 Operating Condition at Power-up / Power-down

Table 4-5: Operating Condition at Power-up / Power-down

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDDH}	V_{DDH} rise time rate	The supply voltage rises from 0 to V_{DDH}.	0	110000	μs/V
	V_{DDH} fall time rate	The supply voltage falls from V_{DDH} to 0.	0	110000	



Note: During power-off, after the LVR generates a low-level reset, a complete power-up sequence must be undergone upon repowering.

4.3.3 VDT Voltage Detection (LVR/LVD)

Unless otherwise specified, V_{DDH} = 5.0 V, T_A = -40~105℃.

Table 4-6: VDT Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
T_J	Junction temperature	-	-40	25	110	℃
I_{OP}	Operating current	-	-	2.5	-	μA
V_{TH0_LVR}	Trigger voltage of LVR	V_{ADJ_LVR} = 0 V_{ADJ_LVR} = 1 V_{ADJ_LVR} = 2 V_{ADJ_LVR} = 3 V_{ADJ_LVR} = 4 V_{ADJ_LVR} = 5 V_{ADJ_LVR} = 6 V_{ADJ_LVR} = 7 V_{ADJ_LVR} = 8 V_{ADJ_LVR} = 9 V_{ADJ_LVR} = 10	Typ * (1 - 1.5%)	1.89 2.1 2.39 2.7 3 3.3 3.6 3.87 4.2 4.48 4.81	Typ * (1 + 1.5%)	V

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{TH1_LVR}	Release voltage of LVR	V_{ADJ_LVR} = 0	Typ * (1 - 1.5%)	2	Typ * (1 + 1.5%)	V
		V_{ADJ_LVR} = 1		2.2		
		V_{ADJ_LVR} = 2		2.5		
		V_{ADJ_LVR} = 3		2.79		
		V_{ADJ_LVR} = 4		3.1		
		V_{ADJ_LVR} = 5		3.38		
		V_{ADJ_LVR} = 6		3.7		
		V_{ADJ_LVR} = 7		3.99		
		V_{ADJ_LVR} = 8		4.29		
		V_{ADJ_LVR} = 9		4.59		
		V_{ADJ_LVR} = 10		4.87		
V_{TH0_LVD}	Trigger voltage of LVD	V_{ADJ_LVD} = 0	Typ * (1 - 1.5%)	1.89	Typ * (1 + 1.5%)	V
		V_{ADJ_LVD} = 1		2.1		
		V_{ADJ_LVD} = 2		2.39		
		V_{ADJ_LVD} = 3		2.7		
		V_{ADJ_LVD} = 4		3		
		V_{ADJ_LVD} = 5		3.3		
		V_{ADJ_LVD} = 6		3.6		
		V_{ADJ_LVD} = 7		3.87		
		V_{ADJ_LVD} = 8		4.2		
		V_{ADJ_LVD} = 9		4.48		
		V_{ADJ_LVD} = 10		4.81		
V_{TH1_LVD}	Release voltage of LVD	V_{ADJ_LVD} = 0	Typ * (1 - 1.5%)	2	Typ * (1 + 1.5%)	V
		V_{ADJ_LVD} = 1		2.2		
		V_{ADJ_LVD} = 2		2.5		
		V_{ADJ_LVD} = 3		2.79		
		V_{ADJ_LVD} = 4		3.1		
		V_{ADJ_LVD} = 5		3.38		
		V_{ADJ_LVD} = 6		3.7		
		V_{ADJ_LVD} = 7		3.99		
		V_{ADJ_LVD} = 8		4.29		
		V_{ADJ_LVD} = 9		4.59		
		V_{ADJ_LVD} = 10		4.87		

Notes:

1. The above simulation results are based on V_{BG08} = 0.8 V.
2. The internal voltage divider resistor is 10 Mohm.

4.3.4 Supply Current Characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, flip speed of I/O pin, location of program in memory, code executed, etc.

Table 4-7: Supply Current Characteristics

Symbol	Description	Test Condition		Min.	Typ.	Max.	Unit
I_{DD}	Operating current	Active mode: V_{DDH} = 5.0 V, T_A = 25℃; all peripherals are disabled, the code runs "while(1){}" in Flash. CLK = 60 MHz		-	4.84	-	mA
		Active mode: V_{DDH} = 5 V, T_A = 25℃; all peripherals are enabled, the code runs "while(1){}" in Flash.	CCLK = 60 MHz	-	7.06	-	mA
			CCLK = 30 MHz	-	4.12	-	mA
			CCLK = 7.5 MHz	-	2.15	-	mA
		Sleep mode: V_{DDH} = 3.3 V, T_A = 25℃		-	2.271	-	mA
		DeepSleep mode: V_{DDH} = 3.3 V; T_A = 25℃		-	41.1	-	μA
		Stop mode: V_{DDH} = 3.3 V; T_A = 25℃		-	37.9	-	μA

4.3.5 Internal Clock Source Characteristics

4.3.5.1 High-speed Internal RC Oscillator (RCH)

Table 4-8: RCH Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{CLKO}	Clock frequency	-	58	60	63	MHz
D	Duty cycle	-	45	50	55	%
t_{SET}	Setup time	-	-	-	20	μs
C_L	Load capacitance	-	-	-	50	fF

4.3.5.2 Low-speed Internal RC Oscillator (RCL)

Table 4-9: RCL Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{CLKO}	Clock frequency	After trimming, T_J = -40℃~125℃	27.8	32.768	36.2	kHz
D	Duty cycle	-	45	50	55	%
t_{SET}	Setup time	-	-	-	0.1	μs
C_L	Load capacitance	-	-	-	50	fF

4.3.6 Wake-up Time from Low-power Mode

Table 4-10: Wake-up Time

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{wakeup}	Time for DeepSleep mode switching to Active mode	Regulator voltage = 2.5 V, T_A = 25℃, 60 MHz	-	13	-	μs

4.3.7 Flash Memory Characteristics

Table 4-11: Flash Memory Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ECflash	Sector endurance	-	100 K	-	-	cycles
RETflash	Data retention	-	10	-	-	year
t_{prog}	Word program time	-	-	-	20	μs
t_{erase}	Sector erase time	-	2	-	5	ms
	Chip erase time	-	20	-	40	ms

Note: Guaranteed by characterization results rather than test in production.

4.3.8 Absolute Maximum Ratings (Electrical Sensitivity)

Using specific measurement methods, the chip is stressed to determine its performance in terms of electrical sensitivity.

4.3.8.1 Electrostatic Discharge (ESD)

Table 4-12: ESD Characteristics

Symbol	Description	Class	Max.	Unit
$V_{ESD(HBM)}$	ESD @ Human Body Model	Class 3B	6000	V
$V_{ESD(CDM)}$	ESD @ Charge Device Model	Class C2	2000	V
$I_{latchup}$	Latch up current	Class IIA	200	mA

4.3.9 I/O Port Characteristics

Table 4-13: I/O Characteristics

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{IL}	Logic low level input current	V_I = 0 V	-1	-	-	μA
I_{IH}	Logic high level input current	V_I = V_{DDH}	-	-	+1	μA
V_O	Output voltage	Output pin being active	0	-	V_{DDH}	V
V_{IH}	Logic high level input voltage	-	0.7 * V_{DDH}	-	-	V
V_{IL}	Logic low level input voltage	-	-	-	0.3 * V_{DDH}	V
V_{hys}	Hysteresis voltage	-	0.1 * V_{DDH}	-	-	V
V_{OH}	Logic high level output voltage	V_{DDH} = 5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	V_{DDH} - 0.8	-	-	V
		V_{DDH} = 3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	2.4	-	-	V
V_{OL}	Logic low level output voltage	V_{DDH} = 5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	-	-	0.5	V

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
		V_{DDH} = 3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	-	-	0.4	V
I_{OH}	Logic high level output current	V_{DDH} = 5 V, normal output in high-drive mode normal output in low-drive mode	- -	16 8	- -	mA
		V_{DDH} = 3.3 V, normal output in high-drive mode normal output in low-drive mode	- -	8 4	- -	mA
I_{OL}	Logic low level output current	V_{DDH} = 5 V, normal output in high-drive mode normal output in low-drive mode	- -	16 8	- -	mA
		V_{DDH} = 3.3 V, normal output in high-drive mode normal output in low-drive mode	- -	8 4	- -	mA
R_{pup} R_{pdn}	Pull up / down current	5 V / 3.3 V	20	-	100	kΩ
C_{IN}	Capacitive impedance	5 V / 3.3 V	-	-	10	pF

4.3.10 ADC Electrical Characteristics

Table 4-14: ADC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
I_{OP}	Operating current	@ f_{ADCCLK} = 30 MHz	-	1	-	mA
Sampling rate	Sampling rate	-	-	1	1.2	MHz
f_{ADCCLK}	ADC clock	-	1.875	32	32	MHz
Input capacitance	-	-	-	7.7	-	pF
SNR @ 30 kHz	Signal-to-noise ratio	-	-	64.87	-	dB
THD @ 30 kHz	Total harmonic distortion	-	-	-69.66	-	dB
DNL[3]	Differential nonlinearity	-	-	+2.36/ -0.87	-	LSB
INL[3]	Integral nonlinearity	-	-	+1.72/ -2.28	-	LSB

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ENOB @ 30 kHz	Effective number of bits	@ Sampling rate = 1.2 MHz	-	10.28	-	Bits

Note: The above data were tested under a 5V power supply. In the CP3 test, a control range of ±25 LSB is set due to equipment errors and other reasons. Higher test accuracy needs to be controlled in the FT test.

4.3.11 Electrical Characteristics of Programmable Gain Amplifier (PGA)

Table 4-15: PGA Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{OP}	Supply voltage	-	2.5	5	5.5	V
A_V	DC voltage gain	SEL_GAIN[2:0] = 000	0.993	1.004	1.014	V/V
		SEL_GAIN[2:0] = 001	1.98	2.007	2.0271	
		SEL_GAIN[2:0] = 010	3.97	4.013	4.054	
		SEL_GAIN[2:0] = 011	7.84	8.002	8.163	
		SEL_GAIN[2:0] = 100	15.66	15.981	16.301	
		SEL_GAIN[2:0] = 101	30.976	31.935	32.894	
		SEL_GAIN[2:0] = 110	61.90	63.816	65.731	
f_{-3dB}	-3 dB bandwidth	SEL_GAIN[2:0] = 000	-	10	-	MHz
		SEL_GAIN[2:0] = 001	-	5	-	
		SEL_GAIN[2:0] = 010	-	2.5	-	
		SEL_GAIN[2:0] = 011	-	1.25	-	
		SEL_GAIN[2:0] = 100	-	0.6	-	
		SEL_GAIN[2:0] = 101	-	0.3	-	
		SEL_GAIN[2:0] = 110	-	0.15	-	
C_L	Load capacitance	-	-	-	5	pF
R_{IN}	Input resistance	SEL_GAIN[2:0] = 000	44.48	55.6	66.72	kohm
		SEL_GAIN[2:0] = 001	66.8	83.5	100.2	
		SEL_GAIN[2:0] = 010	111.28	139.1	166.92	
		SEL_GAIN[2:0] = 011	199.92	249.9	299.88	
		SEL_GAIN[2:0] = 100	377.12	471.4	565.68	
		SEL_GAIN[2:0] = 101	731.6	914.5	1,097.4	

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
		SEL_GAIN[2:0] = 110	1,440	1800	2,160	

Note: Guaranteed by design rather than test in production.

4.3.12 Analog Comparator (COMP) Electrical Characteristics

Table 4-16: COMP Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
I_{OP}	Operating current	-	-	100	-	μA
V_{IC}	Input common voltage	-	0	-	V_{DDH}	V
V_{OS}	Offset voltage	V_{DDH} = 5 V, T_A = 25℃	-	-	10	mV
t_{DR}	Rising edge propagation delay	V_{DDH} = 5 V, V_{ID} = 100 mV	-	10	20	ns
t_{DF}	Falling edge propagation delay	V_{DDH} = 5 V, V_{ID} = -100 mV	-	40	50	ns
V_{HYS}	Hysteresis voltage	HYS<1:0> = 00	-	0	-	mV
		HYS<1:0> = 01	-	10	-	mV
		HYS<1:0> = 10	-	20	-	mV
		HYS<1:0> = 11	-	30	-	mV

Note: Guaranteed by design rather than test in production.

4.4 SIP Pre-driver Electrical Characteristics (UM32MP56-H6U7)

4.4.1 Absolute Maximum Ratings

Table 4-17: Absolute Maximum Ratings

Symbol	Description	Test Condition	Min.	Max.	Unit
V_{B1}, V_{B2}, V_{B3}	High-side bootstrap power supply	-	-0.3	70	V
V_{S1}, V_{S2}, V_{S3}	High-side floating ground terminal	-	V_B-20	V_B + 0.3	V

Symbol	Description	Test Condition	Min.	Max.	Unit
HO1, HO2, HO3	High-side output	-	V_S - 0.3	V_B + 0.3	V
LO1, LO2, LO3	Low-side output	-	-0.3	V_{CC} + 0.3	V
V_{IN}	High-side power supply	-	-0.3	65	V
VCC	Power supply	-	-0.3	20	V

4.4.2 ESD & Latchup Ratings

Table 4-18: ESD & Latchup Ratings

Symbol	Description	Max.	Unit
$V_{ESD(HBM)}$	Human body model (HBM)	2	kV
$I_{Latchup}$	-	150	mA

4.4.3 Typical Parameters

Unless otherwise specified, T_A = 25℃, V_{IN} = 24 V, and load capacitance C_L = 1 nF.

Table 4-19: Typical Parameters

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
V_{IN}	High-voltage input power supply	-	-	-	65	V
I_{VIN}	V_{IN} quiescent current	HIN, LIN floating	-	420	-	μA
I_{BS}	V_{VB} quiescent current	V_{BS} = 12 V, HIN = 0 V or 5 V	-	90	-	μA
I_{lk}	V_S leakage current	V_B = V_S = 60 V	-	0.1	-	μA
V_{B1}, V_{B2}, V_{B3}	High-side bootstrap power supply	-	-0.3	-	65	V
V_{S1}, V_{S2}, V_{S3}	High-side floating ground terminal	-	V_B - 15	-	V_B + 0.3	V
HO, HO2, HO3	High-side output	-	V_S - 0.3	-	V_B + 0.3	V
LO1, LO2, LO3	Low-side output	-	-0.3	-	15	V
V_{CC}	Low-side supply voltage	-	5	-	15	V
V_{SN}	V_S quiescent	V_{BS} = 10 V	-	-	-10	V

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
	negative voltage					
R_{HO}	HO pull-down resistor	-	-	110	-	kΩ
$V_{CC(on)}$	V_{CC} turn-on voltage	-	-	3.8	-	V
$V_{CC(off)}$	V_{CC} turn-off voltage	-	-	3.4	-	V
$V_{B(on)}$	V_B turn-on voltage	-	-	3.5	-	V
$V_{B(off)}$	V_B turn-off voltage	-	-	3.2	-	V
V_G	Gate output voltage	-	-	13	-	V
V_{CC}	V_{CC} output voltage	-	-	12	-	V
V_{DD5}	5V LDO output voltage	-	-	4.95	-	V
I_{VDD5}	5V LDO output current	-	-	100	-	mA
IO+	IO output source current	V_O = 0 V, V_{IN} = V_{IH}, PW ≤ 10 μs	-	+1.5	-	A
IO-	IO output sink current	V_O = 12 V, V_{IN} = V_{IL}, PW ≤ 10μs	-	-1.8	-	A

4.5 SIP Pre-driver Electrical Characteristics (UM32MP56-E6P7)

4.5.1 Absolute Maximum Ratings

Exceeding the absolute maximum ratings may cause permanent damage to the device. All voltage parameter ratings are referenced to GND with an ambient temperature of 25℃.

Table 4-20: Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
V_{cc}	Supply voltage	-0.3	40	V
V_{DD}	LDO output voltage	-0.3	6	
I_{VDD}	LDO output current	-0.3	50	
V_{IN}	Logic output $HIN_{1,2,3}$ & $LIN_{1,2,3}$	-0.3	20	

Symbol	Description	Min.	Max.	Unit
V_{HO}	High-side output voltage $HO_{1,2,3}$	V_{CC} - 15	V_{cc}	
V_{LO}	Low-side output voltage $LO_{1,2,3}$	-0.3	15	

4.5.2 ESD Ratings

Table 4-21: ESD Ratings

Symbol	Description	Max.	Unit
$V_{ESD(HBM)}$	Human body model (HBM)	1	kV
$I_{Latchup}$	-	100	mA

4.5.3 Rated Power

Table 4-22: Rated Power

Symbol	Description	Min.	Max.	Unit
P_D	Package power ($T_A \leq 25$ ℃)	-	1.4	W

4.5.4 Recommended Operating Range

To ensure proper operation, the device shall be used under the following recommended conditions. All voltage ratings are referenced to GND, current parameters take current flowing into the port as positive, and the ambient temperature is 25℃.

Table 4-23: Recommended Operating Range

Symbol	Description	Min.	Max.	Unit
V_{cc}	Low-side supply voltage	5	28	V
I_{VDD}	LDO output current (V_{CC} = 10 V–28 V)	0	40	mA
	LDO output current (V_{CC} = 11 V–28 V)	0	50	mA
$V_{IN,ON}$	Logic input ON threshold voltage for $HIN_{1,2,3}$ and $LIN_{1,2,3}$	2.9	V_{cc}	V
$V_{IN,OFF}$	Logic input OFF threshold voltage for $HIN_{1,2,3}$ and $LIN_{1,2,3}$	0	0.4	V
t_{DT}	Input dead zone between $HIN_{1,2,3}$ and $LIN_{1,2,3}$	0.5	-	μs
f_{IN}	Input signal frequency	0	50	kHz
T_A	Ambient temperature	-40	105	℃

4.5.5 Electrical Characteristics

Unless otherwise specified, T_A = 25℃, $V_{CC1,2}$ = 24 V, and C_L = 1 nF.

4.5.6 Dynamic Parameter Characteristics

Table 4-24: Dynamic Parameter Characteristics

Symbol	Definition	Min.	Typ.	Max.	Unit
t_{ON}	Turn-on propagation delay	-	80	-	ns
t_{OFF}	Turn-off propagation delay	-	30	-	ns
DT	Dead time	-	130	-	ns
t_R	Turn-on rise time	-	300	-	ns
t_F	Turn-off fall time	-	60	-	ns
MT	Delay matching time (t_{ON}, t_{OFF})	-	80	-	ns

4.5.7 Static Parameter Characteristics

Unless otherwise specified, $V_{CC1,2}$ = 24 V, T_A = 25℃. The parameters of V_{IH}, V_{IL} and I_{IN} are referenced to GND, which are accordingly applicable to the input pins $HIN_{1,2,3}$ and $LIN_{1,2,3}$. The parameters of V_O and I_O are referenced to GND, which are accordingly applicable to the output pins $HO_{1,2,3}$ and $LO_{1,2,3}$.

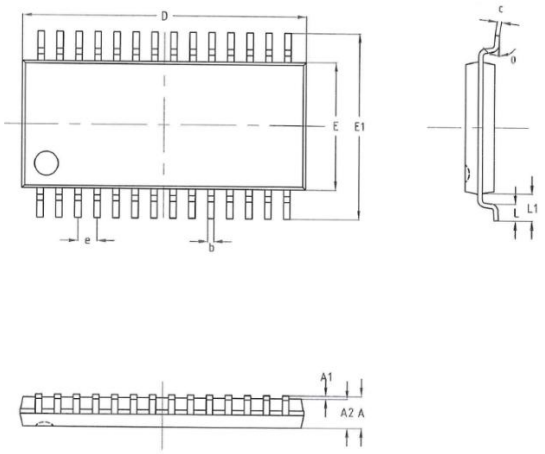
Table 4-25: Static Parameter Characteristics

Symbol	Definition	Min.	Typ.	Max.	Unit
V_{IH}	Logic high level input threshold voltage	2.5	-	-	V
V_{IL}	Logic low level input threshold voltage	-	-	0.8	V
I_{IN+}	Logic “1” input bias current	-	36	100	μA
I_{IN-}	Logic “0” input bias current	-	0	1	μA
$V_{HO,OH}$	HO high-level output voltage	-	V_{cc}	-	V
V_{HO_OL}	HO low-level output voltage	V_{CC} - 11.5	V_{CC} - 10	V_{CC} - 8.5	V
$V_{LO,OH}$	LO high-level output voltage	8.5	10	11.5	V
V_{LO_OL}	LO low-level output voltage	-	0	-	V
I_{O+}	Output high short-circuit pulse current	-	50	-	mA

Symbol	Definition	Min.	Typ.	Max.	Unit
I_{O-}	Output low short-circuit pulse current	-	300	-	mA
V_{CCUV+}	V_{CC} undervoltage positive threshold	3.8	4.5	5	V
V_{CCUV-}	V_{CC} undervoltage negative threshold	3.6	4.3	4.8	V
V_{CCHYS}	V_{CC} undervoltage hysteresis	0.1	0.2	0.4	V
I_{QCC}	V_{CC} quiescent current	0.3	0.5	1.0	mA
V_{DD}	V_{DD} output voltage	4.7	5	5.3	V
T_{SD+}	Thermal-shutdown temperature	-	150	-	℃
T_{SD-}	Recovery temperature after thermal shutdown	-	135	-	℃

5 Package Outline

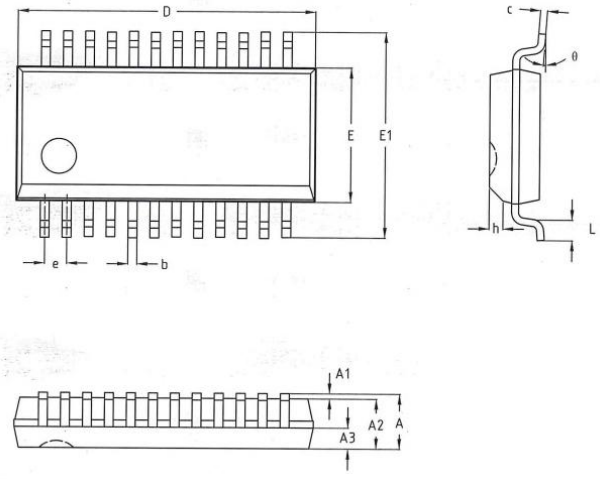
5.1 TSSOP28 (9.7 * 4.4 mm)



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.00
b	0.19	–	0.30
c	0.14	–	0.18
D	9.60	9.70	9.80
E	4.30	4.40	4.50
E1	6.25	6.40	6.55
e	0.65 BSC		
L1	1.00REF		
L	0.45	0.60	0.75
θ	0°	–	8°

Figure 5-1: TSSOP28 Package Outline

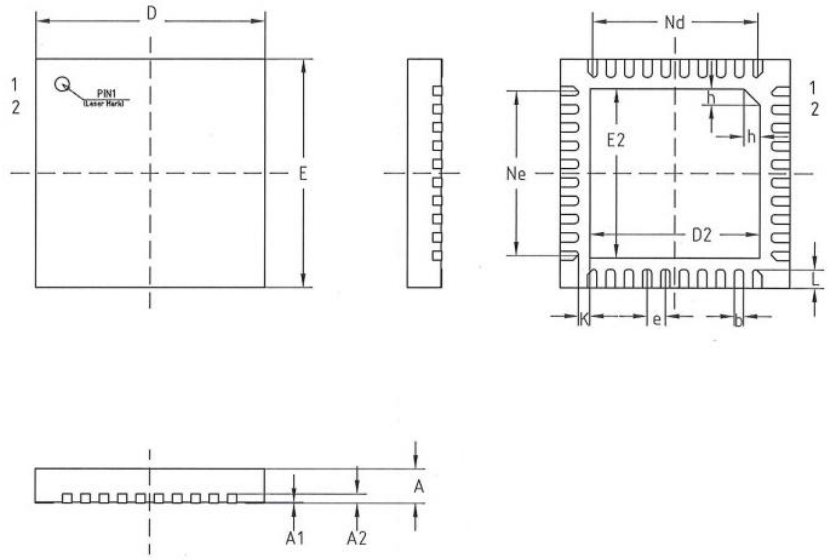
5.2 SSOP24 (8.6 * 3.9 mm)



机械尺寸/mm Dimensions			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	–	–	1.75
A1	0.10	–	0.25
A2	1.35	1.45	1.55
A3	0.60	0.65	0.70
b	0.23	–	0.31
c	0.19	–	0.25
D	8.50	8.60	8.70
E	3.80	3.90	4.00
E1	5.80	6.00	6.20
e	0.635 BSC		
h	0.30	–	0.50
L	0.40	–	0.80
θ	0°	–	8°

Figure 5-2: SSOP24 Package Outline

5.3 QFN40 (5 * 5 mm)



机械尺寸/mm			
字符 SYMBOL	最小值 MIN	典型值 NOMINAL	最大值 MAX
A	0.70	0.75	0.80
A1	–	0.02	0.05
A2	0.203 REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
D2	3.60	3.70	3.80
E	4.90	5.00	5.10
E2	3.60	3.70	3.80
e	0.40 BSC		
K	0.20	0.25	0.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40
Ne	3.60 BSC		
Nd	3.60 BSC		

Figure 5-3: QFN40 Package Outline

6 Revision History

Date	Version	Description
Feb-13-2025	V1.0	Initial release.
Sep-10-2025	V1.0.1	1. Added the section “1.2 Naming Convention”. 2. Updated the maximum main frequency to 60 MHz. 3. Updated TSSOP28 package outline drawing.

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