UNICMICRO 广芯微电子

UM32G130/131

Ultra-low Power 32-bit IoT Processor: ARM®Cortex®-M0+, 64KB eFlash, 8KB SRAM

Product Features

- **Low-power power management system**
  - 1.2 µA @ 3.0 V DeepSleep + RTC mode, with RCL running, and data retention in IO, SRAM and registers
  - 0.9 µA @ 3.0 V Stop mode, with all clocks stopped, and data retention in IO, SRAM and registers
  - 50 µA/MHz @ 3.0 V @ 32 MHz Active mode
  - 3.7 µs fast sleep wake-up system
  - Integrated low-power modules: LPTimer, LPUART, RTC, WDT
  - Built-in ROSC/LDO/POR, no crystal/LDO/ reset circuits required
- **Processor**
  - 32-bit ARM Cortex-M0+, up to 32 MHz
  - Single-cycle hardware multiplier
- **Memory**
  - 8KB SRAM
  - 64KB eFlash
  - 1KB EEPROM
- **GPIO**
  - Up to 29 I/O ports with interrupt capability
  - Configurable drive capability: 16/8 mA
- **Reset and power management**
  - Low voltage detection (LVD), low voltage reset (LVR)
- **Clock**
  - External high-speed crystal oscillator: 4 MHz–24 MHz
  - External low-speed crystal oscillator: 32.768 kHz
  - Internal high-speed clock: 32 MHz
  - Internal low-speed clock: 32.768 kHz
- **Communication interfaces**
  - 2 × LPUARTs, 3 × general-purpose UARTs
  - 2 × SPIs, supporting master/slave mode

QFN32 (4*4mm)
QFN20 (3*3mm)

  - 1 × I2C, supporting master/ lave mode, with a rate of 400 kbps
  - 1 × CAN2.0 A/B protocol interface, with a rate up to 1 Mbps
    (Not supported for UM32G130)
  - Up to 21 × PWM outputs (with 6 pairs of complementary outputs with dead time)
- **Analog peripherals**
  - 1 × 12-bit 1 Msps ADC, with up to 13 channels
  - 1 × operational amplifier (OPA)
  - 3 × analog comparators (COMP)
- **Timers**
  - 1 × 16-bit ATimer, supporting 4 input captures, 3 dead-time complementary PWM outputs and 1 PWM output
  - 3 × 16-bit GTimers, supporting 3 input captures and 3 dead-time complementary PWM outputs
  - 4 × 16-bit BTimers supporting 4 PWM outputs
  - 2 × 32-bit LPTimers, supporting 4 PWM outputs
  - 1 × low-power RTC timer/counter
  - 1 × 32-bit low-power WDT, resettable and interruptible
  - 1 × 18-bit WWDT, resettable and interruptible
- **Security**
  - Anti-copy board to prevent programs in eFlash from being pirated
  - AES (128/192/256)

- CRC16-CCITT hardware acceleration
- 128-bit UUID

- **Hardware acceleration engine**
  - Divider (DIV)
- **Electrical parameters**
  - Operating voltage: 2.5–5.5 V
  - Operating temperature: -40℃–85℃
  - ESD: ±8 kV (HBM)
- **Moisture sensitivity level:** MSL-3
- **Development support**
  - Updating of IAP applications
  - JTAG->SWD mode for online debugging/downloading
  - Complete SDK and EVB HDK
- **Ordering information**

Type	Part No.
64KB Flash	UM32G131-K8U6 (QFN32) UM32G130-F6U6 (QFN20)

Contents

1 Product Introduction

The UM32G130/131 series of chips are 32-bit IoT processor SoC chips developed by Unicmicro based on the ARM Cortex-M0+ core. It features ultra-low power consumption, low pin count and wide operating voltage range, and is primarily aimed at applications in portable sensing and measurement systems and industrial control within the Internet of Things (IoT) industry. To meet the specific application requirements of these scenarios, the chip system employs unique low-power design techniques. It integrates general peripheral communication interfaces (12-bit SAR ADC, UART, SPI, I2C, etc.); sensor interfaces (ADC, OPA, comparator, etc.), ultra-low power module interfaces (LPUART, LPTIMER, WDT, etc.), and hardware algorithm modules (AES, divider, etc.), The chip features high integration, high interference immunity, high reliability and ultra-low power consumption. It has built-in RC oscillators of both high frequency and low frequency, supporting crystal-free applications. It also supports the Keil MDK integrated development environment and allows software development in C and assembly languages.

Applications:

- Industrial IoT applications
- Intelligent transportation, smart cities, smart homes, etc.
- Smart sensor terminal applications such as smart door lock, asset tracking and wireless monitoring
- Battery-powered applications

1.1 Functional Block Diagram

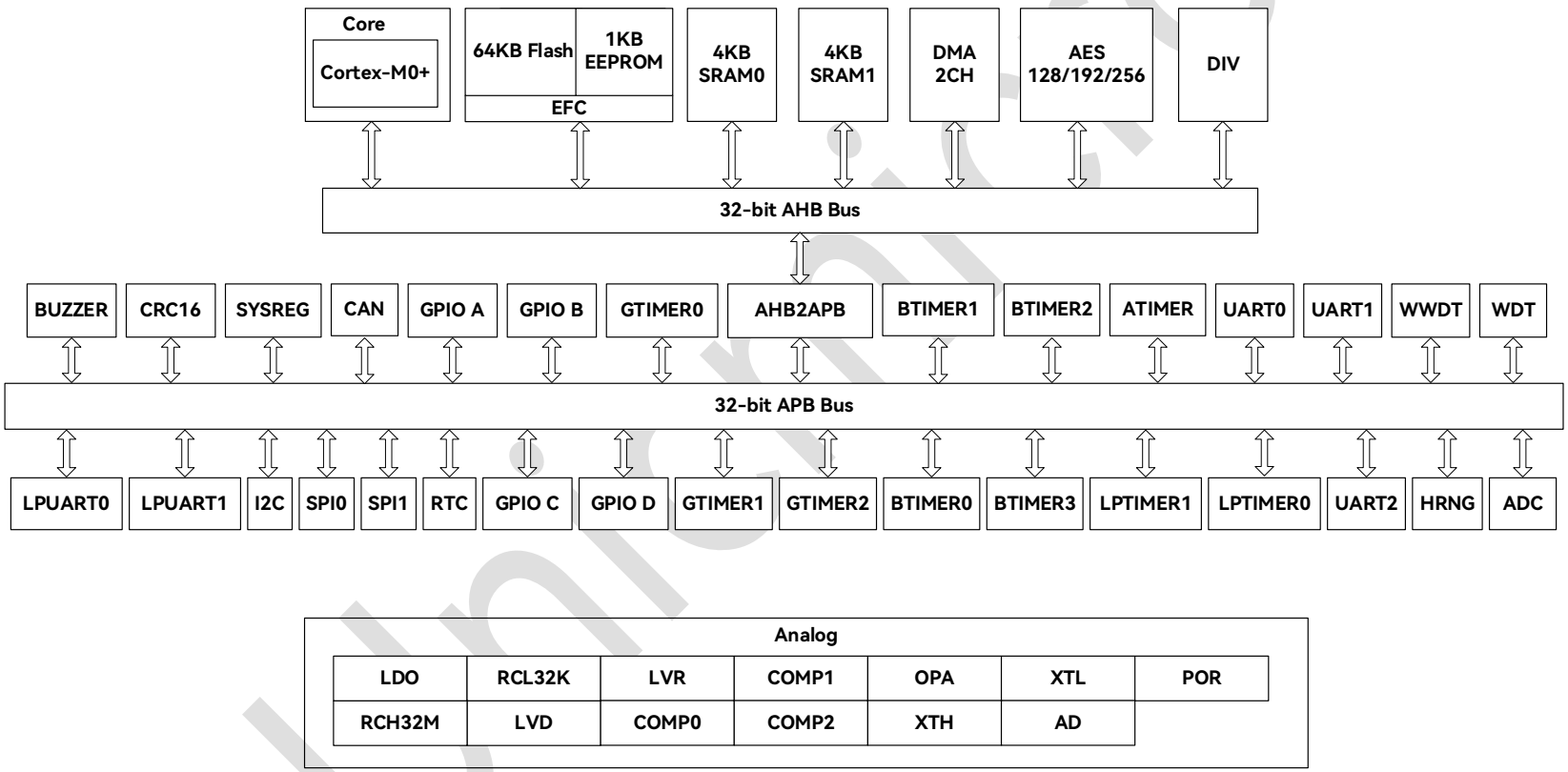


Figure 1-1: Functional Block Diagram

Note: The UM32G130 series does not support CAN.

1.2 Configuration Table

Table 1-1: Configuration Table

Part No.		**UM32G131-K8U6**	**UM32G130-F6U6**
Flash (KB)		64	
EEPROM (KB)		1	
SRAM (KB)		8	
DMA Channels		1 2	
Timers	General-purpose timers	3 (16-bit)	
	Advanced control timer	1 (16-bit)	
	Basic timers	4 (16-bit)	
	SysTick	Yes	
	WDT	1	
	WWDT	1	
	LPTIMER	2	
	RTC	1	
	PWM channels	21	16
Communication interfaces	SPI	2	
	I2C	1	
	UART	3	
	LPUART	2	
	CAN (2.0 B)	1	No
GPIO		29	18
Buzzer		1	
Analog	12-bit ADC Channels	1 13	1 7
	OPA	1	No
	COMP	3	
Hardware encryption/decryption engine	CRC	Yes	
	AES	Yes	
	DIV	Yes	
	RNG	Yes	
Max. CPU frequency		32 MHz	
Operating voltage		2.5–5.5 V	
Operating temperature		Ambient temperature: -40–+85℃	
		Junction temperature: -40–105℃	
Package		QFN32 (4 * 4 mm)	QFN20 (3 * 3 mm)

2 Functional Overview

2.1 Core

The Cortex™ M0+ is a 32-bit two-stage pipelined RISC core embedded with AMBA-Lite interface and nested vectored interrupt controller (NVIC). It features hardware debugging function, Thumb instruction execution and compatibility with other Cortex-M series. The core also incorporates a number of brand-new designs as well as energy-saving and consumption-reducing technologies to improve debugging and tracing capabilities, reduce the number of instructions per clock (IPC), and improve the two-stage pipeline for Flash access. The Cortex M0+ fully supports the integrated Keil & IAR debugger.

2.2 Memory

The chip integrates embedded Flash and embedded SRAM.

2.2.1 Embedded Flash

The chip embeds a 64KB eFlash for storing programs and data.

2.2.2 Embedded SRAM

The on-chip 8KB SRAM allows to maintain data in STOP mode.

2.3 Nested Vectored Interrupt Controller (NVIC)

The nested vectored interrupt controller (NVIC) is a key component of Cortex-M0+. It is tightly coupled with the CPU processor core to achieve low interrupt latency and effective handling of new incoming interrupts, which are prioritized by NVIC connecting the external interrupt signals.

Cortex-M0+ embeds an NVIC which is able to handle up to 32 interrupt request (IRQ) inputs with 4 priority levels, to handle complex logic, as well as to perform real-time control and realize interrupt processing.

All NVIC registers can only be accessed using word transfers. Any attempt to read/write half-words or bytes will result in unpredictable behavior.

This module provides flexible interrupt management with minimal interrupt latency.

2.4 Clock Architecture

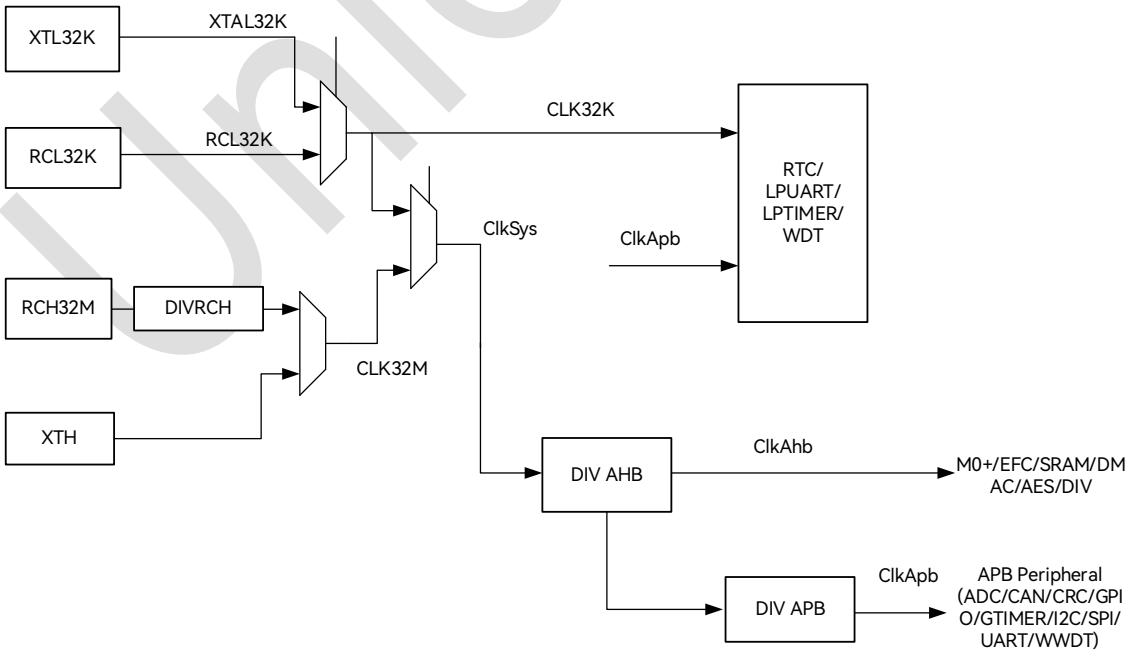


Figure 2-1: Clock Architecture Diagram

The system has four clock sources:

- 32 MHz high-precision internal RCH, used as system clock source
- 4–24 MHz external XTH, used as system clock source
- 32 kHz internal RCL, serving as low-power clock and can be used as system clock source
- 32.768 kHz external XTL, primarily providing RTC and can be used as system clock source

Different clock schemes are required for different operation modes. The system clock source can be selected via configuring the [14:12] bits of the system control register 0 (SYSCTRL0), namely CLK_SEL, CLK_SEL_HF and CLK_SEL_LF. The relationship is shown in the following table.

Table 2-1: System Clock Selection

CLK_SEL	CLK_SEL_HF	System Clock Source
0	0	RCH
0	1	XTH
CLK_SEL	**CLK_SEL_LF**	**System Clock Source**
1	0	RCL
1	1	XTL

2.5 Reset

The system reset sources are listed below.

Table 2-2: System Reset Source

Reset Source	Description
Internal analog POR	Reset all
LVR	
RESETEN	Reset all but CPU DEBUG logic
LOCKUP reset	Reset logics other than EFC and IO related ones
LVD reset	
WDT	
WWDT	
SOFT_RESETN	
Each module reset	Reset the corresponding IP module

2.6 Low-power Mode

In addition to the normal operation mode, there are four low-power modes available for reducing current consumption of the chip: Sleep mode, DeepSleep mode, Stop mode and LPRun mode.

Detailed descriptions are listed in the table below:

Table 2-3: Low-power Modes Summary

Mode	Mode Description	Entry Condition	Exit Condition
Sleep	LDO active power supply; most of CPU (including NVIC) sleeps and WIC does not sleep; the software can disable clocks of various modules.	1. Disable clocks of peripheral modules as required, leaving only the module needed for monitoring the interrupt event. 2. Execute WFI/WFE instructions.	1. CM0+ detects an interrupt or event. 2. Enter the interrupt service routine to clear the interrupt and return. 3. Continue executing subsequent instructions.
DeepSleep	LDO standby power supply; most of CPU (including NVIC) sleeps and WIC does not sleep; the high-speed clock source is disabled and the low-speed clock source RCL is running.	1. Disable clocks of peripheral modules as required, leaving only the module needed for monitoring the interrupt event. 2. Set the DeepSleep register inside CM0+. 3. Execute WFI/WFE instructions.	1. CM0+ detects an interrupt or event. 2. Enter the interrupt service routine to clear the interrupt and return. 3. Continue executing subsequent instructions.
Stop	LDO standby power supply; all system clocks are off.	1. Set the conditions for IO wake-up as required. 2. Set the DeepSleep register inside CM0+. 3. Set the	1. External IO wake-up event occurs. 2. CM0+ detects the interrupt triggered by external IO wake-up event.

Mode	Mode Description	Entry Condition	Exit Condition
		STOPMODE_SEL register in system register. 4. Execute WFI/WFE instructions.	3. Enter the interrupt service routine to clear the interrupt and return. 4. Continue executing subsequent instructions.
LPRun	The system clock is switched to the low-speed clock source RCL or XTL, and LDO enters the low-power mode.	1. Set the SYSCTRL0 register in the system register to switch the system clock to the low-speed clock source RCL or XTL. 2. Set the LDO_SOFT register in the system register to set the LDO into low-power mode.	The system exits LPRUN mode after reset.

2.7 Direct Memory Access Controller (DMA)

Direct memory access (DMA) supports 2-channel data transfer.

The DMA is used to provide high-speed data transfer between peripherals and memory as well as from memory to memory. Data can be quickly moved by DMA without any CPU actions, which keeps the CPU resources free for other operations, thus improving the system efficiency.

Main features:

- Single master
- Controllable data transfer among FLASH, SRAM, SPI0, SPI1, UART1, ADC, GPIOA, LPTIMER and ATIMER modules, where FLASH can only be used as source address.
- Memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral transfers

- Each controller is provided with 2 DMA channels.
- Settable bit width and block length of data transfer
- The block length is up to 32767 words.
- Invariant transfer and incremental transfer of source address Invariant transfer and incremental transfer of destination address
- Support infinite transfer
- Burst transfer supported with configurable burst size of 2/4/8/16

2.8 Universal Asynchronous Receiver Transmitter (UART)

UART is a widely used serial communication interface that supports full-duplex communication. The UART converts parallel data from memory or a processor into serial data for transmission to an external UART receiver, or it converts serial data received from an external UART device into parallel data for the processor. UART supports serial communication with external interface devices.

The chip embeds three UART modules: UART0, UART1 and UART2.

UART0/UART2 comes with an 8-bit 4-level RX FIFO, supporting full-duplex data transfer and serial communication with external interface devices. UART1 comes with a 16-byte FIFO supporting fractional frequency division.

UART0/UART2 main features:

- Providing standard asynchronous communication bits (start bit, parity bit, stop bit)
  - Generating a 1-bit start bit
  - Data bit width of 8 bits
  - 1 parity bit (odd or even), or no parity bit

  - Generating a 1-bit stop bit
  - Bytes transmitted sequentially from LSB to MSB
- 8-bit 4-level RX FIFO, no TX FIFO
- Programmable baud rate (adjustable according to parameter F/D), 2 × 8-bit baud rate registers
- Supporting data communication and error handling interrupt
  - Status bit can be accessed by either polling or interrupt
  - Flags of FIFO non-empty, half-full, full, overflow
  - Parity error flag
- Validity check of start bit
- Supporting transfer at common baud rates such as 9600 bps, 19200 bps and 115200 bps

UART1 main features:

- 16-byte hardware FIFO
- Baud rate supports both integer and fractional division
- 9-bit mode
- CTS/RTS hardware flow control
- Error start bit detection
- Frame interrupt detection
- Programmable bit width, parity and number of stop bits
- DMA operation

2.9 Low-power Universal Asynchronous Receiver Transmitter (LPUART)

The chip is provided with two low-power UART modules LPUART0 and LPUART1, which only require a 32kHz clock to operate and can support data reception at baud rates up to 9600. With extremely low power consumption, LPUART can operate in both Sleep and DeepSleep modes.

Main features:

- Asynchronous data transmission and reception
- Standard UART frame format
  - 1 start bit
  - 7 or 8 data bits
  - Odd parity, even parity or no parity bit
  - 1 or 2 stop bits
- From 300 bps to 9600 bps using a 32.768 kHz XTL clock source
- Programmable data polarity
- Data transfer operable in both Sleep and DeepSleep modes
- Chip wakeup in sleep mode:
  - Wake-up on RXD falling edge interrupt
  - Wake-up on start bit detection
  - Wake-up on completion of receiving 1 byte
  - Wake-up on matching 1 byte of data

2.10 General-purpose Input/Output (GPIO)

GPIO contains general data input and output interfaces, which can be shared with other functional pins, depending on the chip configuration. With these data interfaces, any number of pins can be configured as interrupt signals. The chip is provided with four groups of GPIOs, namely GPIOA, GPIOB, GPIOC and GPIOD, which can be abbreviated as PA, PB, PC and PD respectively. The GPIO registers shall set corresponding bits for their functions. For example, to set the direction of PA1 as output, the control bit[1] of GPIO_DIR shall be set to 1, and the setting of other bits follows this principle, that is, the direction of PAx can be set via the corresponding control bit[x] of GPIO_DIR.

Main features:

- The direction of any I/O port can be configured by software.
- Each GPIO_IN pin can be configured to trigger an interrupt in edge or level mode.

2.11 Advanced Timer (ATIMER)

The advanced timer contains a 16-bit auto-reload counter and a programmable prescaler that can support multiple applications such as input capture, output compare, PWM, complementary PWM with dead-time insertion, etc.

Main features:

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing real-time adjustment of the counter clock frequency division

- 4 independent channels for input capture, output compare, PWM generation, and one-pulse output
- Complementary output with programmable dead-time insertion
- Support cascade between timers
- Repetition counter to update the timer registers only after a given number of cycles of the counter
- Two break pin inputs, comparator break, LVD break, break signal filtering and polarity selection, combinatorial configuration of break signals
- Interrupt or DMA event can be generated in the following cases:
  - Counter overflow/underflow, counter initialization (triggered by software or hardware)
  - Trigger event (counter start, stop, initialization, or count by internal/external trigger)
  - Input capture
  - Output compare
  - Break input
- Support incremental quadrature encoder and Hall sensor

2.12 General-purpose Timer (GTIMER)

There are three 16-bit general-purpose timers GTIMER 0/1/2, with independent interrupt for each. They may be used for a variety of purposes, including measuring the pulse width of input signal (input capture) or generating output waveform (PWM, complementary PWM with dead-time insertion). The counter can count up, down or both up and down with the counter value accessible by software at any time. Each timer is provided with two PWM outputs (optionally

complementary or not) and one input capture.

Main features:

- 16-bit up, down, up/down auto-reload counter
- 16-bit programmable prescaler allowing real-time adjustment of the counter clock frequency division
- Flexible selection of counter clock source
- Channels for input capture, output compare, PWM generation (edge- or center-aligned mode), and one-pulse output
- Support cascade between timers
- Complementary output with programmable dead-time insertion
- Break input to put the PWM output in a settable state
- Interrupt generated on the following events:
  - Update: counter up/down overflow
  - Input capture
  - Output compare
  - Break input
- Synchronization circuit to control the timer

2.13 Basic Timer (BTIMER)

There are four basic timers BTIMER 0/1/2/3 for multiple purposes, including generating PWM output waveform or pulse output. The 16-bit timer/counter counts up with the counter value settable and accessible by software at any time.

Main features:

- 16-bit up auto-reload counter
- 16-bit programmable prescaler allowing real-time adjustment of the counter clock frequency division
- Single channel for PWM output compare and one-pulse output
- Interrupt generated on the following events:
  - UE interrupt generated at counter up overflow
  - Output compare
- Synchronization circuit to control the timer

2.14 Low-power Timer (LPTIMER)

Both LPTIMER0 and LPTIMER1 are 32-bit low-power timer/counter modules. Thanks to the diversity of its clock source, it is able to remain operational with extremely low power consumption in all power modes. Given its capability to run even with no internal clock source, LPTIMER0/1 can be used as an external pulse counter in Sleep mode, and can also be combined with an external input trigger signal to realize the “timeout function” regarding waking up the system from low-power modes.

Main features:

- Independent 32-bit up counter
- 3-bit asynchronous clock prescaler with 8 possible dividing factors (1, 2, 4, 8, 16, 32, 64, 128)
- Selectable clock source:
  - Internal clock source: LSCLK (CLK32K), RCLP (CLK1HZ), PCLK
  - External clock source: LPTIN (with analog filter)
- 32-bit compare / capture register
- 32-bit target value register
- Continuous-/single-shot mode
- Configurable input polarity
- External pulse counting with no clock source
- Externally triggered timeout wakeup from low-power modes
- PWM output

2.15 Inter-integrated Circuit (I2C) Interface

The I2C bus interface handles communications between the microcontroller and the serial I2C bus. The I2C module receives and transmits data, and converts data from serial to parallel, or vice versa. It is connected to the I2C bus via the data pin SDA and the clock pin SCL to control all I2C bus-specific sequencing. This module supports master and slave modes.

Main features:

- Master receive/transmit, slave receive/transmit
- Supporting three operating speeds: standard (up to 100 kbps) / fast (up to 400 kbps) / fast+ (up to 1 Mbps)
- 7-bit and 10-bit addressing modes
- Interrupt polling

2.16 Real-time Clock (RTC)

The real-time clock (RTC) is an independent timer/counter that can provide a time-of-day clock/calendar with programmable alarm interrupts. Alarm clock interrupt is realized by configurable real-time clock counting cycle.

Main features:

- Internal or external 32.768 kHz clock source
- Programmable full perpetual calendar using BCD time
- Periodic wake-up interrupt
- Programmable alarm
- XTLF clock signal can be output from PAD for user calibration
- Digital calibration with precision of ±0.119 ppm
- RTC timer not reset
- Two-channel input edge timestamp function

2.17 Controller Area Network (CAN)

The CAN controller being compliant with CAN2.0A/B protocol can be used in the fields of automotive electronics and industrial control.

Main features:

- Provided with priority and arbitration function
- Message can be received or blocked based on its ID
- Reliable error handling and error detection mechanism
- Message sent can be automatically retransmitted if corrupted
- Node can automatically quit the bus in the case of serious error

2.18 Serial Peripheral Interface (SPI)

The serial peripheral interface (SPI) is a serial synchronous communication means for external devices to exchange data over a single line. The chip provides two SPI modules that can be configured as a master or slave device to enable SPI communication with the outside.

Main features:

- Full-duplex or half-duplex single-data-line serial synchronous transfer
- Master and slave modes
- Programmable clock polarity and phase (modes 0/1/2/3)
- Programmable bit rate
- Slave mode frequency up to f_{sys} / 2

- Transmission complete interrupt flag
- Write collision error flag
- Error detection, protection and interrupt flags in master mode
- Supporting DMA
- 8-byte FIFO depth

2.19 Independent Watchdog Timer (WDT)

The watchdog timer can generate a non-maskable interrupt or a reset when it reaches the given timeout value. It can be used to regain control when the system fails to respond as expected due to software errors or external device failures.

Main features:

- 32-bit downcounter with programmable load
- Independent watchdog timer enabled
- Interrupt generation logic with interrupt masking
- Lockout register for software runaway protection
- Software boot function: reset enable/disable setting in WDT control register
- The register configuration of timer counting can be suspended when the CPU is suspended during debugging.

2.20 System Window Watchdog (WWDT)

The system window watchdog is a watchdog running synchronously with CPU, aiming at monitoring the running status of CPU in real time, so that it can reset CPU in the case of abnormal operation to avoid unpredictable consequences.

Main features:

- 18-bit upcounter with programmable load
- Fault detector inside the system
- Same clock as the system clock
- Monitor software error
- Reset will be triggered by feeding the dog before the window or not feeding the dog after timeout (the effective window for dog feeding is within 50%–100% of the time).
- An early warning interrupt will be triggered when the counter reaches 75% of the overflow time.

2.21 Random Number Generator (RNG)

RNG refers to the random number generator that is capable of delivering random number sequences by writing different random seeds.

2.22 Advanced Encryption and Decryption Algorithm Accelerator (AES)

AES algorithm is a block algorithm. Both the encryption algorithm and the key expansion algorithm adopt nonlinear iterative structure. The decryption algorithm has the same structure as the encryption algorithm except that the round keys are used in reverse order, that is, the decryption round keys are the inverse sequence of the encryption round keys.

Main features:

- Cipher key lengths of 128, 192 or 256 bits
- AES encryption and decryption
- Electronic code book (ECB) and cipher block chaining (CBC) modes
- SWAP mode supported for data input and output, i.e., big-endian/little-endian format configurable

2.23 Divider (DIV)

The implementation goal of the DIV is to support division operations where the divisor does not exceed 32 bits. The divisor can be up to 32 bits, while the dividend can be of any bit length. It is primarily used in applications where the divisor is less than 32 bits.

2.24 Analog-to-digital Converter (ADC)

The 12-bit successive approximation analog-to-digital converter with up to 16 input channels can measure signals from 13 external sources, an internal LDO output and an internal 1/4 VDDH

output. A/D conversion of these channels can be performed in single-shot or continuous scan mode. ADC controller implements the communication between CPU and SAR ADC. The result of ADC conversion is stored in the lower 12 bits of the data register.

Main features:

- Supporting DMA transfer
- 16-bit programmable divider for A/D clock generation
- 12-bit resolution configurable by software for A/D input data with a maximum sampling rate of 1 Msps
- 16-channel ADC input: 13 pin channels, 1 internal LDO input and 1 internal 1/4V_{DDH} input
- Analog ADC can be disabled
- Polling mode and interrupt mode
- Single-shot or continuous scan mode
- Interrupt sources: channel data valid (one interrupt source for each of the 15 channels), FIFO full (32 words), FIFO data level reaches the set value (1 or 16 data items)
- On-chip peripherals can trigger ADC conversion
- ADC voltage input range: 0–V_{ref}
- Optional reference voltage source: chip power supply voltage V_{DDH}, external voltage of IO pin V_{REFIO}

2.25 Operational Amplifier (OPA)

OPA is an operational amplifier with rail-to-rail inputs and class AB output stage. The input and output terminals can be configured into different connections as required. The offset voltage can be trimmed.

Main features:

- One operational amplifier
- Voltage range: 2.5–5.5 V

2.26 Analog Comparator (COMP)

COMP is a hysteresis comparator with rail-to-rail inputs. The input terminal can be configured as required. COMP can be used for voltage comparison, and is provided with two input terminals IN+ and IN-. One of the inputs can be selected as the reference point for comparison, so that the comparator will output low when the voltage at the other input is less than the reference voltage, and high vice versa.

Main features:

- 3 x voltage comparators
- Compare interrupt can be generated

2.27 Security System

2.27.1 UID

Each chip is shipped with a unique 16-byte device identifier, including wafer lot information, chip coordinate information, etc.

2.27.2 CRC16 Hardware Cyclic Redundancy Check

CRC16 is a hardware 16-bit CRC cyclic redundancy check calculation circuit based on the polynomial $G(x) = x^{16} + x^{12} + x^5 + 1$. It can calculate the appropriate CRC result for the communication data based on the initial CRC value preset by the user, and it supports setting the order of input data and the results.

2.28 Debugging and Programming System

The debugging and programming system features are as follows:

- **Embedded debugging system**

  The embedded debugging solution provides a full-featured real-time debugger, compatible with standard and mature debugging and development software such as Keil/IAR, supporting 4 hardware breakpoints and multiple software breakpoints.

- **High security**

  The encrypted embedded debugging solution provides a full-featured real-time debugger.

3 Pin Definition and Description

3.1 Pin Definition

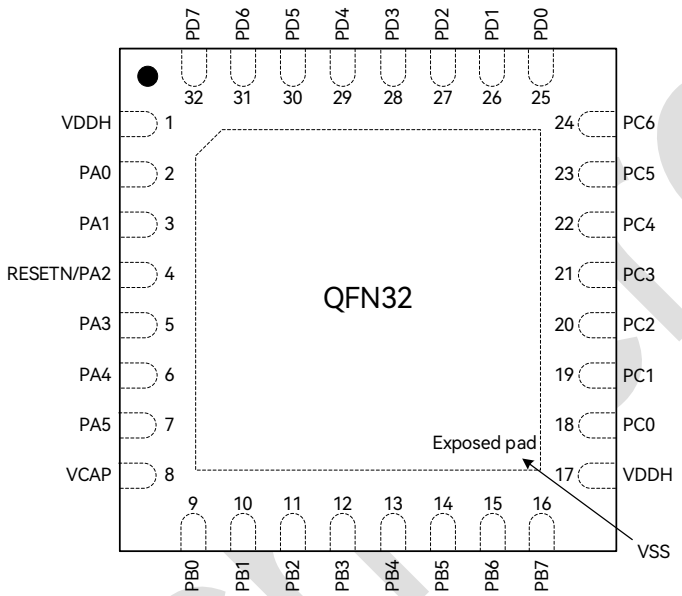


Figure 3-1: QFN32 Pinout Diagram

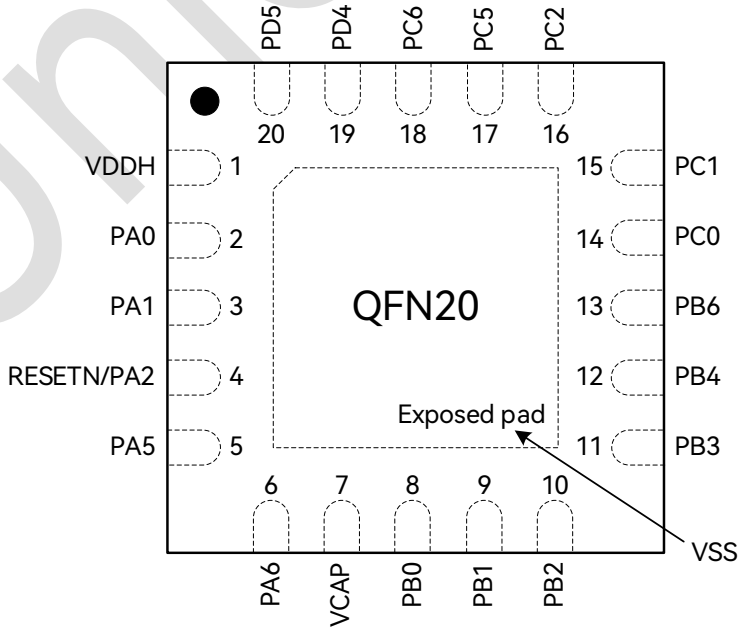


Figure 3-2: QFN20 Pinout Diagram

3.2 Alternate Function

Note: The UM32G130 series does not support CAN.

Table 3-1: Pin Alternate Function

Pin No.		Config	Px_SEL[i+2;i]							
QFN32	QFN20		0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
0	0	VSS	-	-	-	-	-	-	--	-
1/17	1	VDDH	-	-	-	-	-	-	-	-
2	2	XTL_IN	PA0	GTIM2_CHN	RTC_FOUT	SPI0_CSN1	COMP2_OUT	BTIM0_OUT0	UART0_RX	LPUART1_TX
			UART2_TX	UART2_RX	-	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH1	ATIM_BK2
3	3	XTL_OUT	PA1	SPI1_MI1	SPI0_MOSI	LPTIM1_EXT	UART0_RX	GTIM1_CHN	LPUART1_RX	-
			UART2_TX	UART2_RX	ATIM_CH4	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH1N	ATIM_ETR
4	4	RESETN	PA2	-	UART1_RX	UART0_RX	LPUART0_RX	I2C_SCL	I2C_SDA	-
			-	-	-	-	-	-	-	-
5	-	OPA_P0/ AIN10	PA3	UART0_TX	I2C_SDA	SPI0_MI1	LPTIM1_OUT0	BTIM1_OUT0	UART1_RX	SPI1_CSN1
			UART2_TX	UART2_RX	-	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH2	ATIM_BK1
6	-	OPA_N0/ AIN9	PA4	GTIM0_CH	UART1_RX	UART1_CTS	COMP0_OUT	RTC_TAMP0	LPUART0_RX	LPTIM0_IN
			UART2_TX	UART2_RX	BTIM1_OUT1	GTIM1_CH	GTIM2_CH	ATIM_CH2N	ATIM_CH4	CAN_RX
7	5	VREFIO	PA5	GTIM1_CH	LPUART0_TX	UART1_RTS	SPI0_SCK	LPTIM1_IN	SPI1_CSN1	SPI1_MI1
			UART2_TX	UART2_RX	-	GTIM0_CH	GTIM2_CH	ATIM_CH3	LPTIM0_CAP0	LVD_OUT
8	7	VCAP	-	-	-	-	-	-	-	-
9	8	OPA_N1/ AIN7	PB0	GTIM0_CHN	GTIM1_CH	UART1_RX	BUZZER_OUT	SPI1_MOSI	SPI0_MISO/ SPI0_TRI_MO	LPUART0_RX
			UART2_TX	UART2_RX	BTIM0_OUT0	GTIM0_CH	GTIM2_CH	LPTIM1_OUT1	LPUART1_RX	ATIM_CH1N
10	9	OPA_N2/	PB1	SPI1_CSN0	GTIM1_CHN	LPTIM0_EXT	LPTIM0_IN	LPUART0_TX	I2C_SCL	COMP1_OUT

Pin No.		Config	Px_SEL[i+2;i]							
QFN32	QFN20		0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
		AIN6	UART2_TX	UART2_RX	LPTIM0_OUT1	GTIM0_CH	GTIM1_CH	GTIM2_CH	LPTIM1_CAP0	ATIM_CH2
11	10	OPA_O2P/ COMP0_INP1/ COMP1_INP1/ COMP2_INP2/ AIN5	PB2	SPI1_SCK	SPI0_CSN0	GTIM0_CH	SPI0_MOSI	LPTIM1_IN	GTIM2_CHN	ATIM_CH1
			UART2_TX	UART2_RX	LPTIM0_CAP1	GTIM1_CH	GTIM2_CH	ATIM_CH4	LVD_OUT	BTIM0_OUT1
12	11	AIN4	PB3	SPI1_MISO/ SPI1_TRI_MO	COMP0_OUT	LPTIM0_EXT	CAN_RX	RTC_TAMP1	ATIM_CH3	GTIM0_BK
			UART2_TX	UART2_RX	-	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_BK1	-
13	12	AIN3	PB4	SPI0_MOSI	COMP1_OUT	UART1_CTS	SPI1_MOSI	LPTIM0_OUT0	CAN_TX	-
			UART2_TX	UART2_RX	ATIM_ETR	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH1N	-
14	-	AIN2	PB5	GTIM2_CH	SPI1_MISO/ SPI1_TRI_MO	SPI0_MI1	UART1_RTS	GTIM1_CH	LPTIM1_OUT	GTIM1_BK
			UART2_TX	UART2_RX	-	GTIM0_CH	ATIM_CH2N	ATIM_BK1	LPTIM0_OUT1	LPTIM1_CAP1
15	13	AIN1	PB6	LPTIM0_IN	SPI1_MOSI	SPI0_CSN1	GTIM0_CHN	RTC_TAMP1	COMP2_OUT	SPI1_SCK
			UART2_TX	UART2_RX	LPUART1_TX	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH3N	LPTIM1_OUT1
16	-	AIN0	PB7	SPI0_SCK	LPTIM0_OUT0	ATIM_CH1N	RTC_TAMP0	GTIM2_CHN	ATIM_CH4	GTIM2_BK
			UART2_TX	UART2_RX	LPUART1_RX	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH2N	-
18	14	AIN13	PC0	SPI0_MOSI	GTIM0_CH	LPTIM0_IN	ATIM_CH2	CAN_TX	SPI1_MI1	GTIM0_BK
			UART2_TX	UART2_RX	LPTIM1_CAP1	GTIM1_CH	GTIM2_CH	ATIM_CH1	LPTIM1_EXT	ATIM_CH3
19	15	-	PC1	I2C_SCL	UART1_TX	COMP0_OUT	SPI0_MISO/ SPI0_TRI_MO	GTIM1_CH	LPTIM0_OUT0	CAN_RX
			UART2_TX	UART2_RX	ATIM_CH3N	GTIM0_CH	GTIM2_CH	ATIM_CH2	LPTIM0_OUT1	LPTIM1_CAP0
20	16	-	PC2	I2C_SDA	UART1_RX	COMP0_OUT	SPI0_CSN1	GTIM2_CH	LPTIM1_IN	CLKOUT
			UART2_TX	UART2_RX	LPTIM0_OUT1	GTIM0_CH	GTIM1_CH	ATIM_CH3	LPTIM0_CAP1	LVD_OUT

Pin No.		Config	Px_SEL[i+2;i]							
QFN32	QFN20		0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
21	-	XTH_IN/ AIN11	PC3	COMP0_OUT	UART1_CTS	BUZZER_OUT	SPI1_MISO/ SPI1_TRI_MO	GTIM2_CH	UART0_TX	LPTIM0_OUT0
			UART2_TX	UART2_RX	BTIM0_OUT1	GTIM0_CH	GTIM1_CH	ATIM_CH4	ATIM_CH1	LPTIM1_CAP1
22	-	XTH_OUT/ AIN12	PC4	UART1_RTS	SPI1_MOSI	UART0_RX	SPI0_MI1	COMP1_OUT	ATIM_CH3N	LPTIM0_EXT
			UART2_TX	UART2_RX	BTIM1_OUT0	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_ETR	LPTIM1_OUT1
23	17	-	PC5	SWIO	SPI1_SCK	LPTIM0_EXT	I2C_SDA	COMP0_OUT	LPUART0_RX	UART2_TX
			UART2_RX	-	GTIM0_CH	GTIM1_CH	GTIM2_CH	-	-	-
24	18	-	PC6	SWCLK	UART1_TX	SPI1_MISO/ SPI1_TRI_MO	COMP1_OUT	LPUART0_TX	LPTIM0_OUT0	UART2_TX
			UART2_RX	-	GTIM0_CH	GTIM1_CH	GTIM2_CH	-	-	-
25	-	COMP0_INP0	PD0	SPI1_CSN0	GTIM0_CH	UART1_RX	LPTIM1_IN	RTC_TAMP0	GTIM2_CHN	-
			UART2_TX	UART2_RX	BTIM1_OUT1	LPTIM0_OUT1	GTIM1_CH	GTIM2_CH	ATIM_CH3	LPTIM1_CAP0
26	-	COMP0_INN0	PD1	SPI1_SCK	GTIM1_CH	LPTIM1_EXT	SPI1_MI1	-	I2C_SCL	GTIM2_BK
			UART2_TX	UART2_RX	ATIM_CH1N	GTIM0_CH	GTIM2_CH	ATIM_BK2	ATIM_CH2N	LVD_OUT
27	-	COMP1_INN0	PD2	SPI1_MISO/ SPI1_TRI_MO	SPI0_MI1	LPUART1_TX	SPI0_CSN0	LPTIM1_OUT0	COMP2_OUT	GTIM1_BK
			UART2_TX	UART2_RX	BTIM0_OUT0	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_ETR	ATIM_CH3N
28	-	COMP1_INP0	PD3	SPI1_MOSI	LPTIM0_IN	GTIM0_CH	SPI0_CSN1	RTC_TAMP1	LPUART1_RX	CAN_TX
			UART2_TX	UART2_RX	GTIM0_CHN	GTIM1_CH	GTIM1_CHN	GTIM2_CH	ATIM_BK1	LPTIM1_OUT1
29	19	COMP0_INN1/ COMP1_INN1/ COMP2_INP0/ COMP2_INN1	PD4	UART1_TX	I2C_SCL	LPUART0_TX	SPI1_CSN1	SPI0_SCK	GTIM2_CH	LPTIM0_EXT
			UART2_TX	UART2_RX	BTIM0_OUT1	GTIM0_CH	GTIM1_CH	GTIM2_CHN	ATIM_CH1	ATIM_CH2N
30	20	COMP2_INN0/ COMP2_INP1	PD5	I2C_SDA	LPTIM1_IN	UART1_RX	SPI1_MI1	GTIM0_CHN	CAN_RX	LPUART0_RX
			UART2_TX	UART2_RX	ATIM_CH1N	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH2	ATIM_BK2

Pin No.		Config	Px_SEL[i+2;i]							
QFN32	QFN20		0	1	2	3	4	5	6	7
			8	9	10	11	12	13	14	15
31	-	OPA_P2	PD6	UART0_TX	SPI0_MISO/ SPI0_TRI_MO	LPTIM1_EXT	CAN_TX	ATIM_CH1N	SPI0_CSN0	-
			UART2_TX	UART2_RX	BTIM1_OUT0	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_CH3	ATIM_BK1
32	-	OPA_P1	PD7	UART1_TX	SPI1_CSN0	I2C_SCL	SPI0_SCK	GTIM1_CHN	LPTIM1_OUT0	UART0_RX
			UART2_TX	UART2_RX	BTIM1_OUT1	GTIM0_CH	GTIM1_CH	GTIM2_CH	ATIM_ETR	LPTIM0_CAP0
-	6	AIN8	PA6	GTIM2_CH	UART1_TX	SPI0_CSN0	LPUART0_TX	RTC_FOUT	COMP1_OUT	RTC_TAMP1
			UART2_TX	UART2_RX	LPUART1_TX	GTIM0_CH	GTIM1_CH	ATIM_CH3N	ATIM_BK2	CAN_TX

3.3 Pin Description

Table 3-2: Pin Definition

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
0	0	VSS	G	-	-	VSS	The exposed metal pad at the bottom of the chip for connecting to ground.
1/17	1	VDDH	P	-	-	VDDH	External power input to the chip
2	2	PA0	I/O	DI	HZ	PA0	General-purpose digital input/output pin
						GTIM2_CHN	Complementary PWM output signal of GTIMER2
						RTC_FOUT	RTC output signal
						SPI0_CSN1	CSN1 signal of SPI0 (can only be used with SPI0_MI1)
						COMP2_OUT	Output signal of comparator 2
						BTIM0_OUT0	PWM output signal of BTIMER0
						UART0_RX	RX signal of UART0
						LPUART1_TX	TX signal of LPUART1
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTimer1
						GTIM2_CH	Input capture / PWM output signal of GTimer2
						ATIM_CH1	Input capture / PWM output signal of channel 1 of ATIMER
						ATIM_BK2	Break input signal 2 of ATIMER
						XTL_IN	External low-speed crystal oscillator input signal

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
3	3	PA1	I/O	DI	HZ	PA1	General-purpose digital input/output pin
						SPI1_MI1	MISO signal 1 of SPI1, master mode only (can only be used with SPI1_CSN1)
						SPI0_MOSI	MOSI / DC signal of SPI0
						LPTIM1_EXT	External trigger signal of LPTIMER1
						UART0_RX	RX signal of UART0
						GTIM1_CHN	Complementary PWM output signal of GTIMER1
						LPUART1_RX	RX signal of LPUART1
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						ATIM_CH4	Input capture / PWM output signal of channel 4 of ATIMER
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH1N	Complementary PWM output signal of channel 1 of ATIMER
						ATIM_ETR	External trigger signal of ATIMER
						XTL_OUT	External low-speed crystal oscillator output signal
4	4	RESETN	I/O	DI	PU	PA2	General-purpose digital input/output pin
						RESETN (default)	External reset input
						UART1_RX	RX signal of UART1
						UART0_RX	RX signal of UART0

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						LPUART0_RX	RX signal of LPUART0
						I2C_SCL	I2C clock
						I2C_SDA	I2C data
5	-	PA3	I/O	DI	HZ	PA3	General-purpose digital input/output pin
						UART0_TX	TX signal of UART0
						I2C_SDA	I2C data signal
						SPI0_MI1	MISO signal 1 of SPI0, master mode only (can only be used with SPI0_CSN1)
						LPTIM1_OUT0	PWM output signal of channel 0 of LPTIMER1
						BTIM1_OUT0	PWM output signal of channel 0 of BTIMER1
						UART1_RX	RX signal of UART1
						SPI1_CSN1	CSN signal 1 of SPI1 (can only be used with SPI1_MI1)
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH2	Input capture / PWM output signal of channel 2 of ATIMER
						ATIM_BK1	Break input signal 1 of ATIMER
						OPA_P0	OPA P0 input
						AIN10	ADC channel 10
6	-	PA4	I/O	DI	HZ	PA4	General-purpose digital input/output pin

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						UART1_RX	RX signal of UART1
						UART1_CTS	CTS signal of UART1
						COMP0_OUT	Output signal of comparator 1
						RTC_TAMP0	TAMP0 input signal of RTC
						LPUART0_RX	RX signal of LPUART0
						LPTIM0_IN	External clock input signal of LPTIMER0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM1_OUT1	PWM output signal of channel 1 of BTIMER1
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH2N	Complementary PWM output signal of channel 2 of ATIMER
						ATIM_CH4	Input capture / PWM output signal of channel 4 of ATIMER
						CAN_RX	RX signal of CAN
						OPA_N0	OPA N0 input
						AIN9	ADC channel 9
7	5	PA5	I/O	DI	HZ	PA5	General-purpose digital input/output pin
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						LPUART0_TX	TX signal of LPUART0
						UART1_RTS	RTS signal of UART1
						SPI0_SCK	SCK signal of SPI0
						LPTIM1_IN	External clock input signal of LPTIMER1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						SPI1_CSN1	CSN1 signal of SPI1 (can only be used with SPI1_MI1)
						SPI1_MI1	MISO signal 1 of SPI1, master mode only (can only be used with SPI1_CSN1)
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH3	Input capture / PWM output signal of channel 3 of ATIMER
						LPTIM0_CAP0	Input capture signal of channel 0 of LPTIMER0
						LVD_OUT	LVD output signal
						VREFIO	IO input reference power for ADC
8	7	VCAP	-	-	-	VCAP	External capacitance (4.7 μF)
9	8	PB0	I/O	DI	HZ	PB0	General-purpose digital input/output pin
						GTIM0_CHN	Complementary PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						UART1_RX	RX signal of UART1
						BUZZER_OUT	Output signal of buzzer
						SPI1_MOSI	MOSI / DC signal of SPI1
						SPI0_MISO/ SPI0_TRI_MO	MISO signal (used with SPI0_CSN0) or TRI_MO signal of SPI0
						LPUART0_RX	RX signal of LPUART0
						UART2_TX	TX signal of UART2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						UART2_RX	RX signal of UART2
						BTIM0_OUT0	PWM output signal 0 of BTIMER0
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						LPTIM1_OUT1	PWM output signal of channel 1 of LPTIMER1
						LPUART1_RX	RX signal of LPUART1
						ATIM_CH1N	Complementary PWM output signal of channel 1 of ATIMER
						OPA_N1	OPA N1 input
						AIN7	ADC channel 7
10	9	PB1	I/O	DI	HZ	PB1	General-purpose digital input/output pin
						SPI1_CSN0	CSN0 signal of SPI1 (used with SPI1_MISO)
						GTIM1_CHN	Complementary PWM output signal of GTIMER1
						LPTIM0_EXT	External trigger signal of LPTIMER0
						LPTIM0_IN	External clock input signal of LPTIMER0
						LPUART0_TX	TX signal of LPUART0
						I2C_SCL	I2C clock
						COMP1_OUT	Output signal of comparator 1
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						LPTIM0_OUT1	PWM output signal of LPTimer0
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						LPTIM1_CAP0	Input capture signal of channel 0 of LPTIMER1
						ATIM_CH2	Input capture / PWM output signal of channel 2 of ATIMER
						OPA_N2	OPA N2 input
						AIN6	ADC channel 6
11	10	PB2	I/O	DI	HZ	PB2	General-purpose digital input/output pin
						SPI1_SCK	SCK signal of SPI1
						SPI0_CSN0	CSN0 signal of SPI0 (used with SPI0_MISO)
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						SPI0_MOSI	MOSI / DC signal of SPI0
						LPTIM1_IN	External clock input signal of LPTIMER1
						GTIM2_CHN	Complementary PWM output signal of GTIMER2
						ATIM_CH1	Input capture / PWM output signal of channel 1 of ATIMER
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						LPTIM0_CAP1	Input capture signal of channel 1 of LPTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH4	Input capture / PWM output signal of channel 4 of ATIMER
						LVD_OUT	LVD output signal

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						BTIM0_OUT1	PWM output signal of BTIMER0
						OPA_O2P	OPA O2P output
						COMP0_INP1	P1 input signal of comparator 0
						COMP1_INP1	P1 input signal of comparator 1
						COMP2_INP2	P2 input signal of comparator 2
						AIN5	ADC channel 5
12	11	PB3	I/O	DI	HZ	PB3	General-purpose digital input/output pin
						SPI1_MISO/ SPI1_TRI_MO	MISO signal (used with SPI1_CSN0) or TRI_MO signal of SPI1
						COMP0_OUT	Output signal of comparator 0
						LPTIM0_EXT	External trigger signal of LPTIMER0
						CAN_RX	RX signal of CAN
						RTC_TAMP1	TAMP1 input signal of RTC
						ATIM_CH3	Input capture / PWM output signal of channel 3 of ATIMER
						GTIM0_BK	Breaking signal of GTIMER0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_BK1	Break input signal 1 of ATIMER
						AIN4	ADC channel 4
13	12	PB4	I/O	DI	HZ	PB4	General-purpose digital input/output pin
						SPI0_MOSI	MOSI / DC signal of SPI0
						COMP1_OUT	Output signal of comparator 1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						UART1_CTS	CTS signal of UART1
						SPI1_MOSI	MOSI / DC signal of SPI1
						LPTIM0_OUT0	PWM output signal of channel 0 of LPTIMER0
						CAN_TX	TX signal of CAN
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						ATIM_ETR	ETR signal of ATIMER
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH1N	Complementary PWM output signal of channel 1 of ATIMER
						AIN3	ADC channel 3
14	-	PB5	I/O	DI	HZ	PB5	General-purpose digital input/output pin
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						SPI1_MISO/ SPI1_TRI_MO	MISO signal (used with SPI1_CSN0) or TRI_MO signal of SPI1
						SPI0_MI1	MISO signal 1 of SPI0, master mode only (can only be used with SPI0_CSN1)
						UART1_RTS	RTS signal of UART1
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						LPTIM1_OUT0	PWM output signal of channel 0 of LPTIMER1
						GTIM1_BK	Breaking signal of GTIMER1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						ATIM_CH2N	Complementary PWM output signal of channel 2 of ATIMER
						ATIM_BK1	Break input signal 1 of ATIMER
						LPTIM0_OUT1	PWM output signal of channel 1 of LPTIMER0
						LPTIM1_CAP1	Input capture signal of channel 1 of LPTIMER1
						AIN2	ADC channel 2
15	13	PB6	I/O	DI	HZ	PB6	General-purpose digital input/output pin
						LPTIM0_IN	External clock input signal of LPTIMER0
						SPI1_MOSI	MOSI / DC signal of SPI1
						SPI0_CSN1	CSN1 signal of SPI0 (can only be used with SPI0_MI1)
						GTIM0_CHN	Complementary PWM output signal of GTIMER0
						RTC_TAMP1	STAMP1 input signal of RTC
						COMP2_OUT	Output signal of comparator 2
						SPI1_SCK	SCK signal of SPI1
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						LPUART1_TX	TX signal of LPUART1
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						ATIM_CH3N	Complementary PWM output signal of channel 3 of ATIMER
						LPTIM1_OUT1	PWM output signal of channel 1 of LPTIMER1
						AIN1	ADC channel 1
16	-	PB7	I/O	DI	HZ	PB7	General-purpose digital input/output pin
						SPI0_SCK	SCK signal of SPI0
						LPTIM0_OUT0	PWM output signal of channel 0 of LPTIMER0
						ATIM_CH1N	Complementary PWM output signal of channel 1 of ATIMER
						RTC_TAMP0	TAMP0 input signal of RTC
						GTIM2_CHN	Complementary PWM output signal of GTIMER2
						ATIM_CH4	Input capture / PWM output signal of channel 4 of ATIMER
						GTIM2_BK	Breaking signal of GTIMER2
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						LPUART1_RX	RX signal of LPUART1
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH2N	Complementary PWM output signal of channel 2 of ATIMER
						AIN0	ADC channel 0
18	14	PC0	I/O	DI	HZ	PC0	General-purpose digital input/output pin
						SPI0_MOSI	MOSI / DC signal of SPI0

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						LPTIM0_IN	External clock input signal of LPTIMER0
						ATIM_CH2	Input capture / PWM output signal of channel 2 of ATIMER
						CAN_TX	TX signal of CAN
						SPI1_MI1	MISO signal 1 of SPI1, master mode only (can only be used with SPI1_CSN1)
						GTIM0_BK	Breaking signal of GTIMER0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						LPTIM1_CAP1	Input capture signal of channel 1 of LPTIMER1
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH1	Input capture / PWM output signal of channel 1 of ATIMER
						LPTIM1_EXT	External trigger signal of LPTIMER1
						ATIM_CH3	Input capture / PWM output signal of channel 3 of ATIMER
						AIN13	ADC channel 13
19	15	PC1	I/O	DO	-	PC1	General-purpose digital input/output pin
						I2C_SCL	I2C clock
						UART1_TX	TX signal of UART1
						COMP0_OUT	Output signal of comparator 0

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						SPI0_MISO/ SPI0_TRI_MO	MISO signal (used with SPI0_CSN0) or TRI_MO signal of SPI0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						LPTIM0_OUT0	PWM output signal of channel 0 of LPTIMER0
						CAN_RX	RX signal of CAN
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						ATIM_CH3N	Input capture / PWM output complementary signal of channel 3 of ATIMER
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH2	Input capture / PWM output signal of channel 2 of ATIMER
						LPTIM0_OUT1	PWM output signal of channel 1 of LPTIMER0
						LPTIM1_CAP0	Input capture signal of channel 0 of LPTIMER1
20	16	PC2	I/O	DI	-	PC2	General-purpose digital input/output pin
						I2C_SDA	I2C data
						UART1_RX	RX signal of UART1
						COMP0_OUT	Output signal of comparator 0
						SPI0_CSN1	CSN1 signal of SPI0 (can only be used with SPI0_MI1)
						GTIM2_CH	Input capture / PWM output signal of GTIMER2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						LPTIM1_IN	External clock input signal of LPTIMER1
						CLKOUT	Clock output pin
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						LPTIM0_OUT1	PWM output signal of channel 1 of LPTIMER0
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						ATIM_CH3	Input capture / PWM output signal of channel 3 of ATIMER
						LPTIM0_CAP1	Input capture signal of channel 1 of LPTIMER0
						LVD_OUT	LVD output signal
21	-	PC3	I/O	DI	HZ	PC3	General-purpose digital input/output pin
						COMP0_OUT	Output signal of comparator 0
						UART1_CTS	CTS signal of UART1
						BUZZER_OUT	Output signal of buzzer
						SPI1_MISO/ SPI1_TRI_MO	MISO signal (used with SPI1_CSN0) or TRI_MO signal of SPI1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						UART0_TX	TX signal of UART0
						LPTIM0_OUT0	PWM output signal of channel 0 of LPTIMER0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM0_OUT1	PWM output signal 1 of BTIMER0

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						ATIM_CH4	Input capture / PWM output signal of channel 4 of ATIMER
						ATIM_CH1	Input capture / PWM output signal of channel 1 of ATIMER
						LPTIM1_CAP1	Input capture signal of channel 1 of LPTIMER1
						XTH_IN	XTH input control:
						AIN11	ADC channel 11
22	-	PC4	I/O	DI	HZ	PC4	General-purpose digital input/output pin
						UART1_RTS	RTS signal of UART1
						SPI1_MOSI	MOSI signal of SPI1
						UART0_RX	RX signal of UART0
						SPI0_MI1	MISO signal 1 of SPI0, master mode only (can only be used with SPI0_CSN1)
						COMP1_OUT	Output signal of comparator 1
						ATIM_CH3N	Input capture / PWM output complementary signal of channel 3 of ATIMER
						LPTIM0_EXT	External trigger signal of LPTIMER0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM1_OUT0	PWM output signal 0 of BTIMER1
						GTIM0_CH	Input capture / PWM output signal of GTIMER0

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_ETR	External trigger signal of ATIMER
						LPTIM1_OUT1	PWM output signal of channel 1 of LPTIMER1
						XTH_OUT	XTH output signal
						AIN12	ADC channel 12
23	17	PC5	I/O	DI	PU	PC5	General-purpose digital input/output pin
						SWIO (default)	Data signal of JTAG SWD
						SPI1_SCK	SCK signal of SPI1
						LPTIM0_EXT	External trigger signal of LPTIMER0
						I2C_SDA	I2C data
						COMP0_OUT	Output signal of comparator 0
						LPUART0_RX	RX signal of LPUART0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
24	18	PC6	I/O	DI	PU	PC6	General-purpose digital input/output pin
						SWCLK (default)	Clock signal of JTAG SWD
						UART1_TX	TX signal of UART1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						SPI1_MISO/ SPI1_TRI_MO	MISO signal (used with SPI1_CSN0) or TRI_MO signal of SPI1
						COMP1_OUT	Output signal of comparator 1
						LPUART0_TX	TX signal of LPUART0
						LPTIM0_OUT0	PWM output signal of channel 0 of LPTIMER0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
25	-	PD0	I/O	DI	HZ	PD0	General-purpose digital input/output pin
						SPI1_CSN0	CSN0 signal of SPI1 (used with SPI1_MISO)
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						UART1_RX	RX signal of UART1
						LPTIM1_IN	External clock input signal of LPTIMER1
						RTC_TAMP0	TAMP0 input signal of RTC
						GTIM2_CHN	Input capture / PWM output complementary signal of GTIMER2
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM1_OUT1	PWM output signal 1 of BTIMER1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						LPTIM0_OUT1	PWM output signal of channel 1 of LPTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH3	Input capture / PWM output signal of channel 3 of ATIMER
						LPTIM1_CAP0	Input capture signal of channel 0 of LPTIMER1
						COMP0_INP0	INP0 input signal of comparator 0
26	-	PD1	I/O	DI	HZ	PD1	General-purpose digital input/output pin
						SPI1_SCK	SCK signal of SPI1
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						LPTIM1_EXT	External trigger signal of LPTIMER1
						SPI1_MI1	MISO signal 1 of SPI1, master mode only (can only be used with SPI1_CSN1)
						I2C_SCL	I2C clock
						GTIM2_BK	Breaking signal of GTIMER2
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						ATIM_CH1N	Input capture / PWM output complementary signal of channel 1 of ATIMER
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM2_CH	Input capture / PWM output signal of GTIMER2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						ATIM_BK2	Break input signal 2 of ATIMER
						ATIM_CH2N	Complementary PWM output signal of channel 2 of ATIMER
						LVD_OUT	LVD output signal
						COMP0_INN0	INN0 input signal of comparator 0
27	-	PD2	I/O	DI	HZ	PD2	General-purpose digital input/output pin
						SPI1_MISO/ SPI1_TRI_MO	MISO signal (used with SPI1_CSN0) or TRI_MO signal of SPI1
						SPI0_MI1	MISO signal 1 of SPI0, master mode only (can only be used with SPI0_CSN1)
						LPUART1_TX	TX signal of LPUART1
						SPI0_CSN0	CSN0 signal of SPI0 (used with SPI0_MISO)
						LPTIM1_OUT0	PWM output signal of channel 0 of LPTIMER1
						COMP2_OUT	Output signal of comparator 2
						GTIM1_BK	Breaking signal of GTIM1
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM0_OUT0	PWM output signal 0 of BTIMER0
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_ETR	External trigger signal of ATIMER

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						ATIM_CH3N	Complementary PWM output signal of channel 3 of ATIMER
						COMP1_INN0	INN0 input signal of comparator 1
28	-	PD3	I/O	DI	HZ	PD3	General-purpose digital input/output pin
						SPI1_MOSI	MOSI signal of SPI1
						LPTIM0_IN	External clock input signal of LPTIMER0
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						SPI0_CSN1	CSN1 signal of SPI0 (can only be used with SPI0_MI1)
						RTC_TAMP1	TAMP1 input signal of RTC
						LPUART1_RX	RX signal of LPUART1
						CAN_TX	TX signal of CAN
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						GTIM0_CHN	Input capture / PWM output complementary signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM1_CHN	Input capture / PWM output complementary signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_BK1	Break input signal 1 of ATIMER
						LPTIM1_OUT1	PWM output signal of channel 1 of LPTIMER1
						COMP1_INP0	INP0 input signal of comparator 1

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
29	19	PD4	I/O	DI	HZ	PD4	General-purpose digital input/output pin
						UART1_TX	TX signal of UART1
						I2C_SCL	I2C clock
						LPUART0_TX	TX signal of LPUART0
						SPI1_CSN1	CSN1 signal of SPI1 (can only be used with SPI1_MI1)
						SPI0_SCK	SCK signal of SPI0
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						LPTIM0_EXT	External trigger signal of LPTIM0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM0_OUT1	PWM output signal 1 of BTIMER0
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CHN	Input capture / PWM output complementary signal of GTIMER2
						ATIM_CH1	Input capture / PWM output signal of channel 1 of ATIMER
						ATIM_CH2N	Complementary PWM output signal of channel 2 of ATIMER
						COMP0_INN1	INN1 input signal of comparator 0
						COMP1_INN1	INN1 input signal of comparator 1
						COMP2_INP0	INP0 input signal of comparator 2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						COMP2_INN1	INN1 input signal of comparator 2
30	20	PD5	I/O	DI	HZ	PD5	General-purpose digital input/output pin
						I2C_SDA	I2C data
						LPTIM1_IN	External clock input signal of LPTIMER1
						UART1_RX	RX signal of UART1
						SPI1_MI1	MISO signal 1 of SPI1, master mode only (can only be used with SPI1_CSN1)
						GTIM0_CHN	Input capture / PWM output complementary signal of GTIMER0
						CAN_RX	RX signal of CAN
						LPUART0_RX	RX signal of LPUART0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						ATIM_CH1N	Complementary PWM output signal of channel 1 of ATIMER
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH2	Input capture / PWM output signal of channel 2 of ATIMER
						ATIM_BK2	Break input signal 2 of ATIMER
						COMP2_INN0	INN0 input signal of comparator 2
						COMP2_INP1	INP1 input signal of comparator 2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
31	-	PD6	I/O	DI	HZ	PD6	General-purpose digital input/output pin
						UART0_TX	TX signal of UART0
						SPI0_MISO/ SPI0_TRI_MO	MISO signal (used with SPI0_CSN0) or TRI_MO signal of SPI0
						LPTIM1_EXT	External trigger signal of LPTIMER1
						CAN_TX	TX signal of CAN
						ATIM_CH1N	Complementary PWM output signal of channel 1 of ATIMER
						SPI0_CSN0	CSN0 signal of SPI0 (used with SPI0_MISO)
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM1_OUT0	PWM output signal 0 of BTIMER1
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_CH3	Input capture / PWM output signal of channel 3 of ATIMER
						ATIM_BK1	Break input signal 1 of ATIMER
						OPA_P2	OPA P2 input
32	-	PD7	I/O	DI	HZ	PD7	General-purpose digital input/output pin
						UART1_TX	TX signal of UART1
						SPI1_CSN0	CSN0 signal of SPI1 (used with SPI1_MISO)
						I2C_SCL	I2C clock

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						SPI0_SCK	SCK signal of SPI0
						GTIM1_CHN	Input capture / PWM output complementary signal of GTIMER1
						LPTIM1_OUT0	PWM output signal of channel 0 of LPTIMER1
						UART0_RX	RX signal of UART0
						UART2_TX	TX signal of UART2
						UART2_RX	RX signal of UART2
						BTIM1_OUT1	PWM output signal 1 of BTIMER1
						GTIM0_CH	Input capture / PWM output signal of GTIMER0
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						ATIM_ETR	External trigger signal of ATIMER
						LPTIM0_CAP0	Input capture signal of channel 0 of LPTIMER0
						OPA_P1	OPA P1 input
-	6	PA6	I/O	DI	HZ	PA6	General-purpose digital input/output pin
						GTIM2_CH	Input capture / PWM output signal of GTIMER2
						UART1_TX	TX signal of UART1
						SPI0_CSN0	CSN signal 0 of SPI0 (used with SPI0_MISO)
						LPUART0_TX	TX signal of LPUART0
						RTC_FOUT	RTC output signal
						COMP1_OUT	Output signal of comparator 1
						RTC_TAMP1	TAMP1 input signal of RTC
						UART2_TX	TX signal of UART2

Pin No.		Pin Name	IO Type	Reset Status		Pin Type	Functional Description
QFN32	QFN20			DIR	PU PD		
						UART2_RX	RX signal of UART2
						LPUART1_TX	TX signal of LPUART1
						GTIM0_CH	Input capture / PWM output signal of GTIM0ER
						GTIM1_CH	Input capture / PWM output signal of GTIMER1
						ATIM_CH3N	Complementary PWM output signal of channel 3 of ATIMER
						ATIM_BK2	Break input signal 2 of ATIMER
						CAN_TX	TX signal of CAN
						AIN8	ADC channel 8

Notes:

- A—analog signal; D—digital signal; I—input; O—output; G—ground; P—power; PU—pull up; PD—pull down; HZ—high impedance state.
- The UM32G130 series does not support CAN.

4 Electrical Characteristics

4.1 Test Condition

Unless otherwise specified, all voltages are referenced to V_{ss}.

4.1.1 Minimum and Maximum Values

Unless otherwise specified, all products are tested on the production line at T_A=25℃. The maximum and minimum values support the worst-case environmental temperature, supply voltage, and clock frequency as specified.

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3Σ).

4.1.2 Typical Value

Unless otherwise specified, typical data are measured based on T_A = 25 ℃ and V_{DDH} = 3.3 V. They are given only as design guidelines.

4.1.3 Typical Curve

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

4.1.4 Power Supply Scheme

The chip supports single power supply and VBAT backup power supply. It requires an external operating supply voltage between 2.5 V and 5.5 V, and a digital circuit operating voltage generated by the built-in LDO.

The system power supply scheme is shown below.

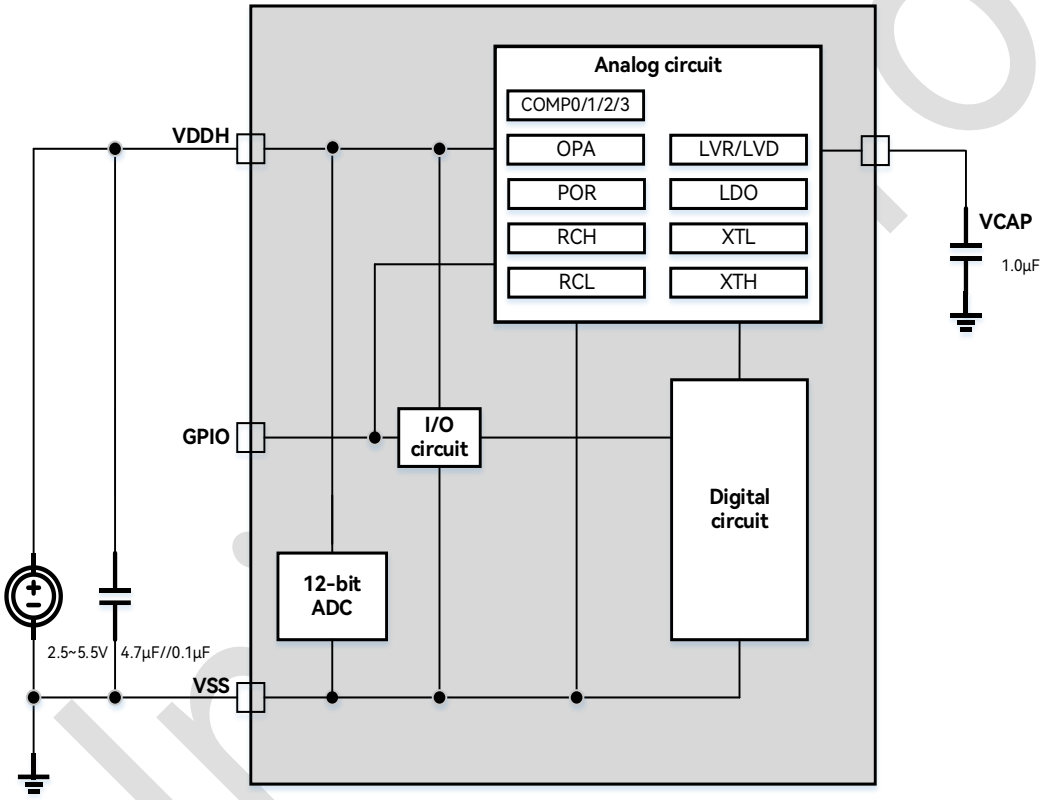


Figure 4-1: Block Diagram of Power Supply Scheme

4.2 Absolute Maximum Ratings

Stresses above the absolute maximum ratings listed in Table 4-1, Table 4-2 and Table 4-3 may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4-1: Voltage Characteristics

Symbol	Description	Min.	Max.	Unit
V_{DDH} – V_{SS}	External main supply voltage(1)	-0.3	6.0	V
V_{IN}	Input voltage on the pin(2)	V_{SS} – 0.3	V_{DDH} + 0.3	
$\|\Delta V_{DDx}\|$	Voltage difference between different supply pins	-	50	mV
$\|V_{SSX} - V_{SS}\|$	Voltage difference between different ground pins	-	50	

Notes:

1. All main power (V_{DDH}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.

2. V_{IN} shall not exceed its maximum value. Refer to Table 4-2 for current characteristics.

Table 4-2: Current Characteristics

Symbol	Description	Max. (1)	Unit
I_{VDDH}	Total current through the V_{DDH-} power line (supply current)(1) (3)	200	mA
I_{VSS}	Total current through the V_{SS} ground line (output current)(1) (3)	200	
I_{IO}	Output sink current on any I/O and control pin	12	
	Output current on any I/O and control pin	-12	
$I_{INJ(PIN)}$(2)	Injection current on NRST pin	-5	
	Injection current on other pins	±5	

Notes:

1. All main power (V_{DDH}) and ground (V_{SS}) pins must always be connected to the external power supply, in the permitted range.

2. A positive injection is induced by $V_{IN} > V_{DDH}$, and a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ maximum must always be respected. Refer to Table 4-1 for the maximum allowed injected current values.

3. When the maximum current occurs, the maximum voltage drop of V_{DDH} is allowed to be $0.1V_{DDH}$.

Table 4-3: Thermal Characteristics

Symbol	Description	Value	Unit
T_{stg}	Storage temperature range	-55~+150	℃
T_J	Maximum junction temperature	105	℃

4.3 Operating Condition

Static parameter table (applicable temperature range: T_A = -40℃~85℃).

4.3.1 General Operating Condition

Table 4-4: General Operating Condition

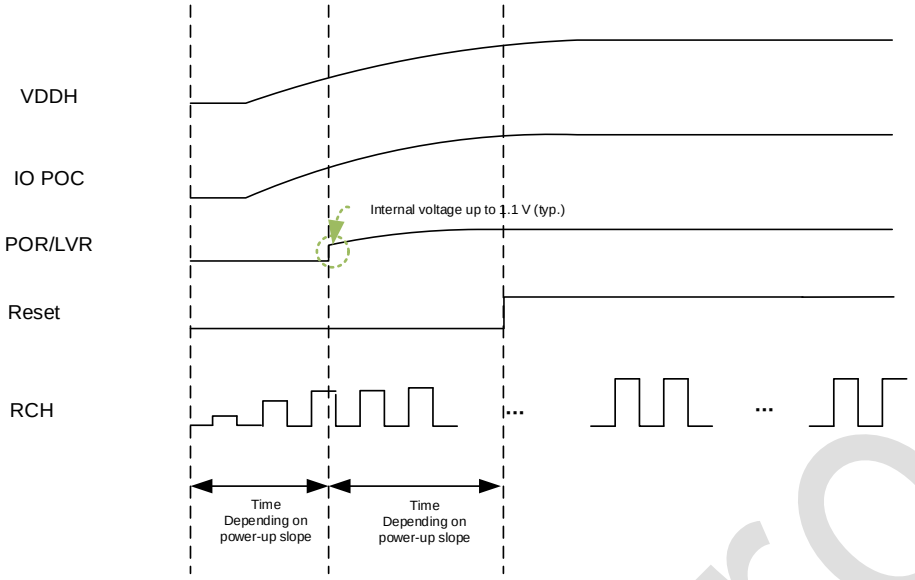
Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{HCLK}	Internal AHB clock frequency	-	0	32	32	MHz
f_{PCLK}	Internal APB clock frequency	-	0	32	32	
V_{DDH}	Standard operating voltage	-	2.5	-	5.5	V
T_A	Ambient temperature	-	-40	-	85	℃
f_{sys}	System frequency	-	0.1	-	32	MHz
T_J	Junction temperature range	-	-40	-	105	℃

*: When f_{sys} is lower than 2 MHz, Flash can only fetch and execute code, but cannot erase or write.

4.3.2 Operating Condition at Power-up / Power-down

Table 4-5: Operating Condition at Power-up / Power-down

Symbol	Parameter	Condition	Min.	Max.	Unit
t_{VDDH}	V_{DDH} rise time rate	The supply voltage rises from 0 to V_{DDH}.	0	110000	μs/V
	V_{DDH} fall time rate	The supply voltage falls from V_{DDH} to 0.	0	110000	



Note: In the case of low-voltage reset occurs during power-down, the whole power-up process shall be experienced after powering up again.

4.3.3 VDT Voltage Detection (LVR/LVD)

Unless otherwise specified, V_{DDH} = 3.3 V, T_A = -40~85℃.

Table 4-6: Low Voltage Detection (LVR) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVR}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVR}	Detection threshold	Deepsleep mode	-	2.11	-	V
		Active mode	-	2.20	-	V

Table 4-7: Low Voltage Detection (LVD) Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{IN_LVD}	Input detection voltage range	-	0	-	V_{DD}	V
V_{LVD}	Detection threshold	ADJ_LVD<2:0>=000	-	4.39	-	V
		ADJ_LVD<2:0> =001		3.95		
		ADJ_LVD<2:0>=010		3.59		
		ADJ_LVD<2:0>=011		3.29		
		ADJ_LVD<2:0>=100		3.04		
		ADJ_LVD<2:0>=101		2.82		
		ADJ_LVD<2:0>=110		2.63		
		ADJ_LVD<2:0>=111		2.46		
I_{VDD}	Current consumption	-	-	2.06	-	mA

4.3.4 Supply Current Characteristics

Current consumption is a comprehensive indicator of various parameters and factors, including operating voltage, ambient temperature, I/O pin load, product software configuration, operating frequency, flip speed of I/O pin, location of program in memory, code executed, etc.

Table 4-8: Supply Current Characteristics

Symbol	Description	Test Condition		Min.	Typ.	Max.	Unit
I_{DD}	Operating current	Active mode: V_{DDH} = 3.3 V, T_A = 25 ℃; all peripherals are disabled, the code runs "while(1){}" in Flash. CCLK = 32 MHz		-	1.56	-	mA
		Active mode: V_{DDH} = 3.3 V/5 V, T_A = 25 ℃; all peripherals are enabled, the code runs "while(1){}" in Flash.	CCLK = 16 MHz	-	1.59	-	mA
			CCLK = 4 MHz	-	0.52	-	mA
			CCLK = 2 MHz	-	0.34	-	mA
		Sleep mode: V_{DDH} = 3.3 V, T_A = 25 ℃		-	0.41	-	mA
		DeepSleep mode: V_{DDH} = 3.3 V; T_A = 25℃		-	1.2	-	μA
		Stop mode: V_{DDH} = 3.3 V; T_A = 25℃		-	0.9	-	μA
		LPRun mode: V_{DDH} = 3.3 V; T_A = 25℃; all IP clocks except RTC are disabled.		-	4.6	-	μA

4.3.5 External Clock Source Characteristics

4.3.5.1 High-speed External Clock Source (XTH)

Table 4-9: XTH Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{OSC_IN}	Frequency range	-	2.0	16	24	MHz
t_{SU}	Clock setup time	-	-	-	0.5	ms
I_{VDD}	Current consumption	-	-	0.2	-	μA
I_{lk}	Leakage current	-	-	1	-	nA

Notes:

1. The resonator characteristics are given by the crystal/ceramic resonator manufacturer.

2. Guaranteed by design rather than test in production.

4.3.5.2 Low-speed External Clock Source (XTL)

Table 4-10: **XTL Characteristics**

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{XTL_IN}	Oscillator frequency	-	-	32.768	-	kHz
$t_{SU(XTL)}$	Startup time	V_{DDH} is stabilized	-	-	2	s
I_{DD}	Operating current	-	-	200	-	nA
$C_{L1/CL2}$	External capacitance	-	-	12	-	pF

4.3.6 Internal Clock Source Characteristics

4.3.6.1 High-speed Internal RC Oscillator (RCH)

Table 4-11: RCH Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{HSI}	Clock frequency	T_A = -40℃~85℃	32 * (1 - 2%)	32	32 * (1 + 2%)	MHz
Duty	Duty cycle	f_{HSI} = 32 MHz	45	50	55	%
t_{SU}	Clock setup time	-	-	3	6	μs
I_{VDD}	Current consumption	-	-	80	-	μA

4.3.6.2 Low-speed Internal RC Oscillator (RCL)

Table 4-12: RCL Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
f_{LSI}	Clock frequency	-	32.768 * (1 - 5%)	32.768	32.768 * (1 + 5%)	kHz
Duty	Duty cycle	-	45	50	55	%
t_{SU}	Clock setup time	-	-	-	100	μs
I_{VDD}	Current consumption	-	-	260	-	nA

4.3.7 Wake-up Time from Low-power Mode

Table 4-13: Wake-up Time

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
t_{wakeup}	Time for DeepSleep mode switching to Active mode	Regulator voltage = 2.5 V, T_A = 25℃, 32 MHz	-	8	-	μs

4.3.8 Flash Memory Characteristics

Table 4-14: Flash Memory Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
ECflash	Sector endurance	-	20 K	-	-	cycles
RETflash	Data retention	-	10	-	-	year
t_{prog}*	Word program time	-	-	-	20	μs
t_{erase}*	Sector erase time	-	15		18	ms
	Chip erase time	-	20	-	40	ms

Note: Guaranteed by characterization results rather than test in production.

*: The parameters t_{prog} and t_{erase} are measured at room temperature and a typical frequency of 32 MHz.

4.3.9 Absolute Maximum Ratings (Electrical Sensitivity)

Using specific measurement methods, the chip is stressed to determine its performance in terms of electrical sensitivity.

4.3.9.1 Electrostatic Discharge (ESD)

Table 4-15: ESD Characteristics

Symbol	Description	Class	Max.	Unit
$V_{ESD(HBM)}$	ESD @ Human Body Mode	Class 3B	8000	V
$V_{ESD(CDM)}$	ESD @ Charge Device Mode	Class C2	1000	V
$I_{latchup}$	Latch up current	Class IIA	200	mA

4.3.10 I/O Port Characteristics

Table 4-16: I/O Characteristics

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{IL}	Logic low level input current	V_I = 0 V	-1	-	-	μA
I_{IH}	Logic high level input current	$V_I = V_{DDH}$	-	-	+1	μA
V_O	Output voltage	Output pin being active	0	-	V_{DDH}	V
V_{IH}	Logic high level input voltage	-	0.7*V_{DDH}	-	-	V
V_{IL}	Logic low level input voltage	-	-	-	0.3*V_{DDH}	V
V_{hys}	Hysteresis voltage	-	0.1*V_{DDH}	-	-	V
V_{OH}	Logic high level output voltage	V_{DDH} = 5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	V_{DDH}-0.8	-	-	V
		V_{DDH} = 3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	2.4	-	-	V
V_{OL}	Logic low level output voltage	V_{DDH} = 5 V, normal output of I_{Load} = 16 mA in high-drive mode and I_{Load} = 8 mA in low-drive mode.	-	-	0.5	V
		V_{DDH} = 3.3 V, normal output of I_{Load} = 8 mA in high-drive mode and I_{Load} = 4 mA in low-drive mode.	-	-	0.4	V

Symbol	Description	Test Condition	Min.	Typ.	Max.	Unit
I_{OH}	Logic high level output current	V_{DDH} = 5 V, output in high-drive mode output in low-drive mode	 - -	 16 8	 - -	mA
		V_{DDH} = 3.3 V, output in high-drive mode output in low-drive mode	 - -	 8 4	 - -	mA
I_{OL}	Logic low level output current	V_{DDH} = 5 V, output in high-drive mode output in low-drive mode	 - -	 16 8	 - -	mA
		V_{DDH} = 3.3 V, output in high-drive mode output in low-drive mode	 - -	 8 4	 - -	mA
R_{pup} R_{pdn}	Pull up / down current	5 V / 3.3 V	20	-	100	kΩ
C_{IN}	Input capacitance	5 V / 3.3 V	-	-	10	pF

4.3.11 ADC Electrical Characteristics

Table 4-17: ADC Electrical Characteristics

Symbol	Description	Condition	Min.	Typ.	Max.	Unit
V_{ADCIN}	ADC input voltage	-	0	-	V_{DDH}	V
V_{REF}	ADC reference voltage	-	0	-	V_{DDH}	V
I_{ADC}	-	-	-	0.9	-	mA
C_{ADCIN}	ADC input capacitance	-	-	4	-	pF
f_{ADCCLK}	ADC clock frequency	-	0.01	0.5	1	MHz
$t_{ADCCONV}$	Conversion time	-	16	16	20	cycle
ENOB	-	-	9.5	10	10.4	bit
DNL	Differential non-linearity	-	-	±1.5	±3	LSB
INL	Integral non-linearity	-	-	±2	±4	LSB

Notes:

- Guaranteed by design rather than test in production.
- In the CP3 test, a control range of ±25 LSB is set due to machine errors and other reasons.

  Higher testing accuracy needs to be controlled during the FT test.

4.3.12 Operational Amplifier (OPA) Characteristics

Table 4-18: OPA Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDH}	Operating voltage	-	2.5	-	5.5	V
T_A	Ambient temperature	-	-40	-	85	℃
I_{DDA}	Operating current	-	-	0.7	-1	mA
C_{MIR}	Common mode input range	-	0	-	V_{DDH}	V
V_{OS}	Offset voltage	Untrimmed	-	-	10	mV
		After trimming	-	1	-	mV
R_{LOAD}	Load resistance	-	10	-	-	kΩ
C_{LOAD}	Load capacitance	-	-	-	20	pF

Note: Guaranteed by design rather than test in production.

4.3.13 Analog Comparator (COMP) Electrical Characteristics

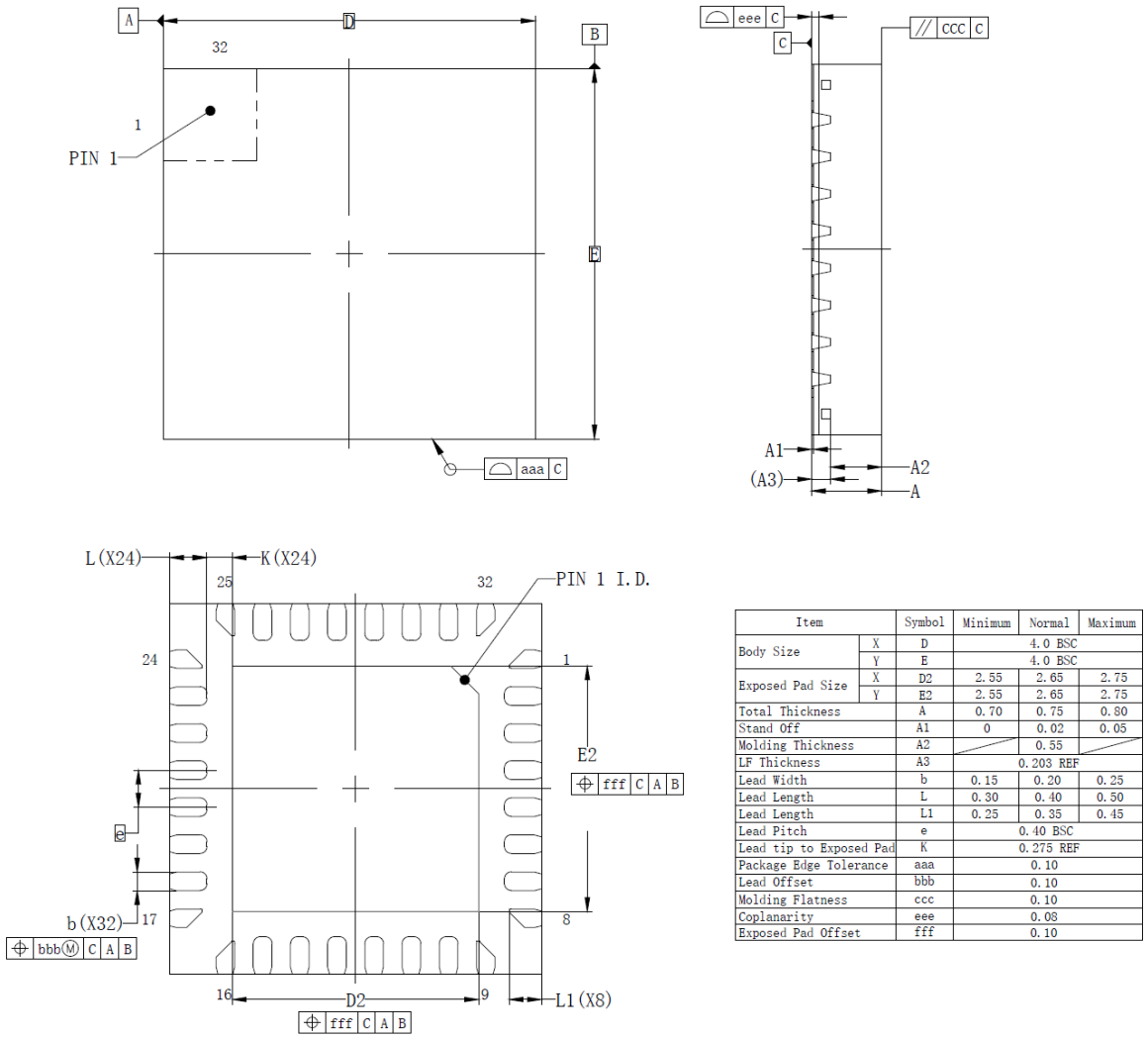
Table 4-19: ACMP Electrical Characteristics

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{DDH}	Analog supply voltage	-	2.5	-	5.5	V
V_{IN}	Input voltage range	-	0	-	V_{DDH}	V
t_{START}	Comparator startup time	V_{ID} = 50 mV	-	0.3	-	μs
t_{DR}	Rising edge propagation delay	V_{ID} = 50 mV	-	0.4	-	μs
t_{DF}	Falling edge propagation delay	V_{ID} = -50 mV	-	0.5	-	μs
V_{OFFSET}	Offset voltage	–	-	±1	±5	mV
V_{hys}	Hysteresis voltage	-	-	0	-	mV
I_{DDA}	Operating current	-	-	4	5	μA

Note: Guaranteed by design rather than test in production.

5 Package Outline

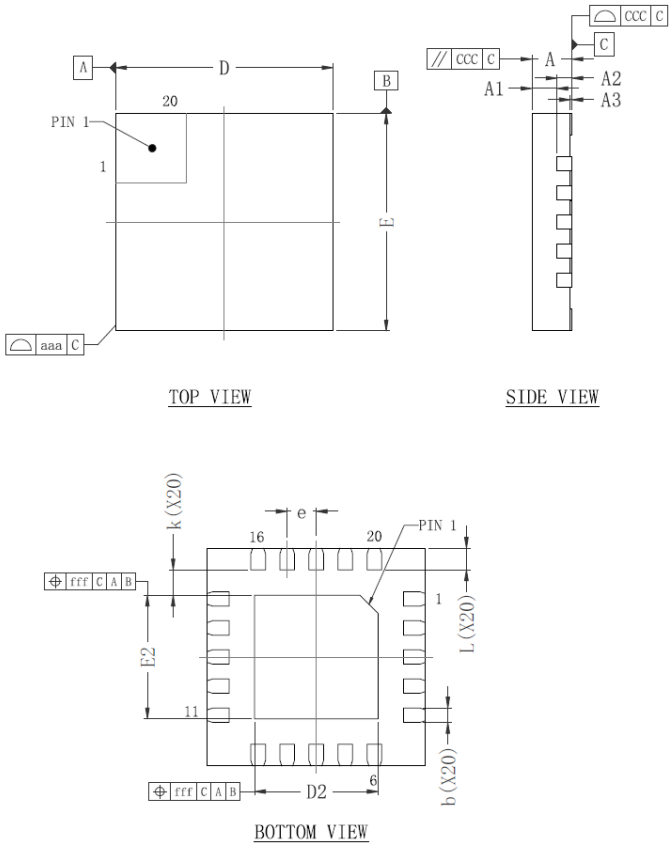
5.1 QFN32 (4 * 4 mm)



Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		4.0 BSC	
	Y	E		4.0 BSC	
Exposed Pad Size	X	D2	2.55	2.65	2.75
	Y	E2	2.55	2.65	2.75
Total Thickness		A	0.70	0.75	0.80
Stand Off		A1	0	0.02	0.05
Molding Thickness		A2		0.55	
LF Thickness		A3		0.203 REF	
Lead Width		b	0.15	0.20	0.25
Lead Length		L	0.30	0.40	0.50
Lead Length		L1	0.25	0.35	0.45
Lead Pitch		e		0.40 BSC	
Lead tip to Exposed Pad		K		0.275 REF	
Package Edge Tolerance		aaa		0.10	
Lead Offset		bbb		0.10	
Molding Flatness		ccc		0.10	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.10	

Figure 5-1: QFN32 Package Outline

5.2 QFN20 (3 * 3 mm)



Item		Symbol	Minimum	Normal	Maximum
Body Size	X	D		3.0 BSC	
	Y	E		3.0 BSC	
Exposed Pad Size	X	D2	1.6	1.7	1.8
	Y	E2	1.6	1.7	1.8
Total Thickness		A	0.5	0.55	0.6
Molding Thickness		A1		0.4	
LF Thickness		A2		0.152 REF	
Stand Off		A3	0	0.02	0.05
Lead Width		b	0.15	0.2	0.25
Lead Length		L	0.2	0.3	0.4
Lead Pitch		e		0.4 BSC	
The space from terminals of lead to exposed pad		k		0.35 REF	
Package Edge Tolerance		aaa		0.1	
Lead Offset		bbb		0.07	
Molding Flatness		ccc		0.1	
Coplanarity		eee		0.08	
Exposed Pad Offset		fff		0.1	

Figure 5-2: QFN20 Package Outline

6 Revision History

Date	Version	Description
Mar-13-2023	V1.0	Initial release.
Apr-03-2023	V1.1	1. Deleted information related to TSSOP28 package. 2. Deleted the model corresponding to UM32G130 64KB EFlash. 3. Modified the number of COMP into 3 on the homepage. 4. Deleted signals regarding COMP3. 5. Added the total number of supported PWMs on the homepage.
Apr-12-2023	V1.2	1. Updated the QFN20 package outline. 2. Updated the pin signals for QFN20 in the tables of alternate function and pin description.
May-08-2023	V1.3	Modified the description “decremental” in WWDT chapter into “incremental”.
Aug-07-2023	V1.4	1. Modified the temperature range on the homepage. 2. Updated CDM parameters.
Oct-16-2023	V1.4.1	1. Updated the maximum junction temperature of the chip. 2. Updated the chapter of Electrostatic Discharge (ESD).
Mar-05-2024	V1.4.2	1. Updated the Flash of UM32G130-F6U6 to 64 KB. 2. Updated the configuration table. 3. Updated the f_{LSI} clock frequency value. 4. Updated the DNL and INL values in the section “ADC Electrical Characteristics”.
Apr-08-2024	V1.5	1. Deleted models UM32G131-E8U6 (QFN24), UM32G131-F8U6 (QFN20), UM32G130-K6T6 (LQFP32), UM32G131-K8T6 (LQFP32), UM32G130-K6U6 (QFN32), and UM32G130-E6U6 (QFN24) and related information. 2. Update the number of OPAs for UM32G130-F6U6 in the configuration table. 3. Deleted descriptions regarding Boot. 4. Deleted descriptions regarding ISP.
Nov-26-2024	V1.5.1	Updated the typical value of V_{LVD} in “Table 6-1: Low Voltage Detection (LVD) Characteristics”.
Mar-10-2025	V1.5.2	Regarding “Table 4-14: FLASH Memory Characteristics”, modified the min. sector erase time from 2 to 15 and the max. from 5 to 18; and added test conditions for t_{prog} and t_{erase}.

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