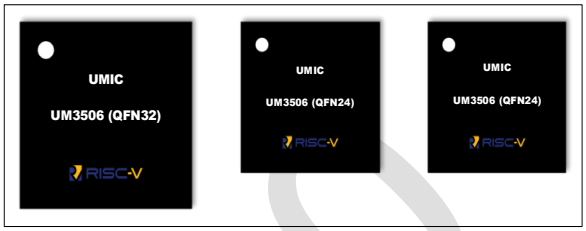
UM3506 Series

PD Plus SoC：RISC-V RV32IMC，256KB Flash，8KB SRAM，PD3.1

Product Feature



- **PD/TYPE-C**
  - Type-C R1.4, Power delivery 3.0/3.1 Spec. (TID: 2465), support upgrade
  - Internal TCPM+TCPC architecture, integrated TCPC-like front end block, support CC detection and control circuit，BMC PHY etc.
  - SRC/SNK/DRP mode, configurable CS and Rd
  - 2 pair DP/DM signal for charge protocol (BC1.2, QC etc.)
  - VBUS DISCHARG
  - DEAD BATTERY
  - PPS (Programming power supply)
  - FRS (Fast role swap)
  - Extended message of 260Bytes
  - OCP, OVP
- **Core**
  - 32Bit RISC-V core，frequency 33MHz
  - RV32IMC
  - I-CACHE for acceleration
- **Memory**
  - 8KB SRAM
  - 256KB Flash
- **Timer**
  - 1 sysTick Timer
  - 3 * 32bit General purpose timer
  - 1 32bit low power WDT
  - PWM Timer，6 channel
- **Clock and Peripherals**
  - Internal 4M ROSC+PLL
  - 2 * UART, UART0 shared for ICP program
  - 2 * I2C, master/slave mode，fast mode, 1Mbps
  - 1 SPI：Master/slave，3 chip sel.
  - Up to 32 GPIO
  - 2 DMA，DMA0 for PD, DMA1
  - 16 channel 12bit SAR ADC
  - Low Side CSA
  - TL431-Based VBUS Regulation (for SRC only)
- **Power**
  - Input：3.3V~24V
  - HVLDO
  - POR/BOD
  - TEMP：-40°C ~85°C
  - ESD Protection：2KV（HBM）
- **Complete USB PD/Type-C software library，Keep continuously**
  - SRC, SNK, DRP (SRC/SNK)
  - PD3.0, PD3.1 EPR
  - Support PD Packet Chunk mode and long 260Bytes mode
  - DR swap, PR swap
  - VCONN swap
  - Vendor-defined message
  - Optional PPS, AVS
  - Optional Extend message (Battery, Manufactory, Country, Status etc.)
  - Optional authentication message
  - Flexible policy management

1. Product Description

UM3506 SoC chip target at latest USB interface solution which complies with USB Power Delivery Rev. 3.0/3.1 and Type-C Rev1.4 specifications. it provides a flexible programmable architecture that allows for continuous evolution of specification and wide range functionality extension beyond PD application.

UM3506 SoC chip internally structured in TCPM/TCPC layered architecture to achieve a complete PD/Type-C system, including operating as source, sink, or DRP, depending on the customer application. The SoC chip integrates one native TCPC-like front end which including essential digital logic and analog circuits for Type-C interface detection and control, dead-battery power-up, packet BMC Encoding/Decoding in PD PHY layer, and timing-critical functions in PD Protocol layer.

UM3506 SoC chip also integrates innovative RISC-V ISA based 32bit MCU core as centralized universal TCPM processor. The optimized RISC-V core incorporate on-chip Flash/SRAM memories, enhanced peripherals and extensively system resource to implements the upper layer protocol of PD specification in proven software package. In additional, it enables flexibility to manage power policy, extension to customized functionalities on control and interactive in one PD plus differentiation system.

UM3506 SoC chip also integrates more system level function module to reduces board BOM material requirement. Customer can easily deploy the USB PD/Type-C system in various system products, greatly shorten the development cycle and cost.

Application Scenario：

- Power Adapter, Power Bank
- Notebook, PC
- Printer, Projector
- Monitor, Smart TV
- Type-C docking

2. Function Description

2.1. Function block

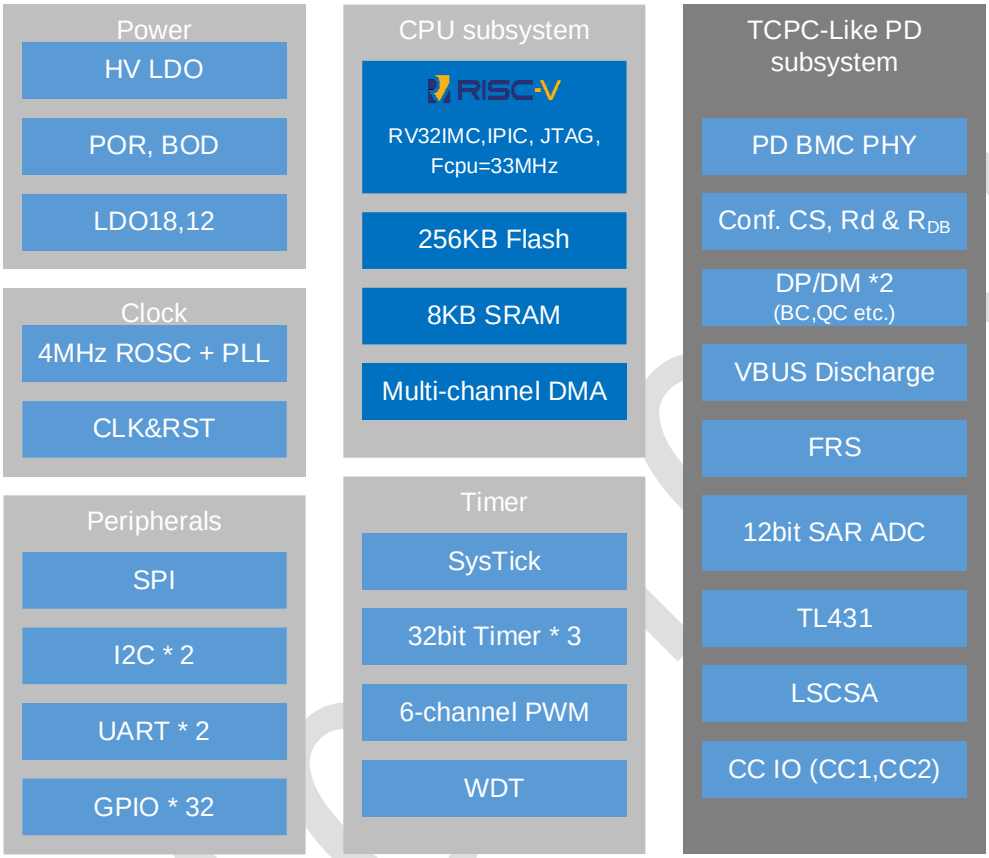


Figure 2-1 UM3506 Block Diagram

2.2. MCU Sub-system

This MCU subsystem includes a high-performance RISC-V MCU core, on-chip memory for programming and data buffer, extensively system resource for USB PD plus application such as system policy and board management.

RISC-V CORE

RISC-V is a free and open instruction set architecture (ISA) enabling a new era of processor innovation through open standard collaboration. It has been developed to provide a low-cost platform that meets the needs of embedded MCU implementation.

The UM3506 device embeds an optimized RISC-V core for power and area as part of the 32-bit MCU subsystem, which execute RV32I base instruction set with M and C extensions.

The RISC-V core in UM3506 device is load-store architecture, where only load and store instructions access memory and arithmetic instructions only operate on integer registers. The core provides a 32-bit user address space that is byte-addressed and little endian. The execution environment will define what portions of the address space are legal to access.

The UM3506 device embed RISC-V core and are compatible with all open-source RISC-V tools and software.

For more information about the RISC-V core, pls. refer to the related reference manual.

On chip flash memory

The UM3506 device embeds a flash module with up to 256KBytes high-density flash, a flash accelerator, tightly coupled to the CPU to improve average access times from the flash block.

On chip SRAM

The UM3506 device embeds up to 8 Kbytes of embedded SRAM accessed (read/write) at CPU clock speed with 0 wait states.

General DMA

The UM3506 device embeds 1 general DMA. The general-purpose DMA manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers.

The general DMA support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

DMA can be used with the main peripherals: UART, SPI, CC.

Memory Map

The following show the illustrative view of the system memory map for the core.

Table 2-1: Memory Map

Memory Space Address	Functional Block
0x4000_0D00 --- 0x4000_0D08	SPI Flash indirect access control registers
0x4000_0C00 --- 0x4000_0C2C	GPIO Port1 registers
0x4000_0B00 --- 0x4000_0B2C	GPIO Port0 registers
0x4000_0A00 --- 0x4000_0A0C	SPI registers
0x4000_0900 --- 0x4000_0920	PWM registers
0x4000_0800 --- 0x4000_0818	Second I2C registers
0x4000_0700 --- 0x4000_0718	I2C registers
0x4000_0600 --- 0x4000_0620	Secondary UART registers
0x4000_0500 --- 0x4000_0520	UART registers
0x4000_0000 --- 0x4000_00FF	PD register
0x6000_0000 --- 0x6000_1FFF	8KB Memory for Data RAM and PD buffer

0x0000_0000 --- 0x00FF_FFFF	Maximum 16 MB Code Size

Watch Dog Timer

The purpose of the watchdog is to reset the controller if software fails to periodically service it within a programmable time window.

General-purpose Timer

The UM3506 device includes three 32-bit counter/timers. The counter/timer is designed to count cycles of the system derived clock. It can optionally generate interrupts or perform other actions at specified timer values, based on three match registers.

The first two counter/timers also includes up to two capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

PWM Timer (2xfcpu)

The UM3506 device includes PWM generator to support 6 channel PWM signals.

2.3. TCPC-like PD Sub-system

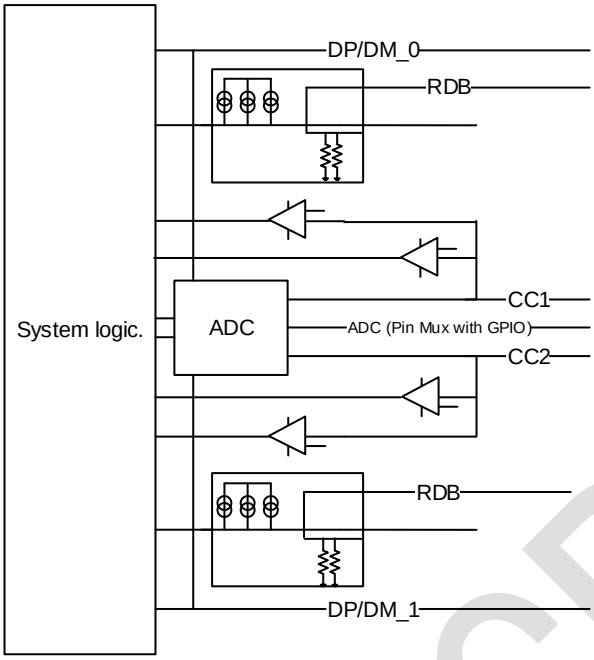
The UM3506 device internally structured in TCPM/TCPC architecture for USB PD native application. It embeds a hardware based TCPC-like PD block which provides a set of commands and register interface for the integrated RISC-V MCU core.

The integrated PD block implements USB PD PHY layer and HW intensive protocol layer functions, work along with integrated RISC-V core can handle all functions for Type-C attach/de-attach detection, plug orientation detection, host to device connection, VCONN support, and VBUS configuration. It also provides a USB PD TX/RX line driver and BMC transceiver which allows USB PD negotiation and alternative mode through the integrated RISC-V MCU.

This block includes essential Type-C detect and control circuit, PD protocol digital logic, in additional high-resolution ADC, a current sense amplifier, a high-voltage regulator, OVP, OCP, and supply switch blocks. This PD block also includes all ESD required and supported on the Type-C port.

TYPE-C Detect/Control Circuit

Figure 2-2 Type-C Controller Block



UM3506 Type-C detect circuit features including：

- Support configurable CS and Rd termination for SRC, SNK, DRP mode
- Support multiple channel ADC for CC circuit detection and VBUS monitor
- Support standard CC channel, 1.05~1.20V voltage level
- Support VBUS_EN and VBUS_DISCHARGE
- Support VCONN sourcing control
- Support OVP/OCP protection
- Support FRS Signal detection and control
- Support 2 pair DP/DM for charger detect

Table 2-2 Current Source termination

SRC advertisement	Current source to VDD	Accuracy
Default USB Power	80 uA ±20%	±20 %
1.5 A at 5 V	180 uA	±8 %
3.0 A at 5 V	330 uA	±8 %

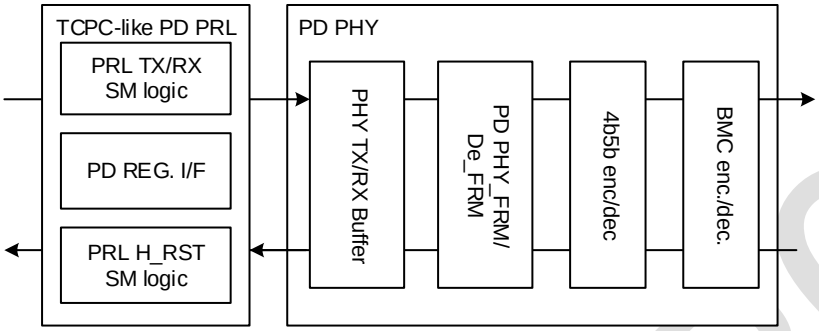
Table 2-3 Pull-down Rd termination

SNK implementation	Rd value	Accuracy
Default USB Power	5.1k	±10 %

PD PRL/PHY Layer

The USB-PD Physical Layer consists of a transmitter and receiver that communicate BMC-encoded data over the CC channel based on the PD 3.0 standard. All communication is half-duplex. The Physical Layer or PHY practices collision avoidance to minimize communication errors on the channel.

Figure 2-3 PD Controller Block



UM3506 implements USB PD PHY layer function as follows:

- Bi-phase Mark Coding/Decoding
- 4B5B Line coding/Decoding
- CRC computation and checking
- Slew rate controlled IO
- Bit transmission and data recovery

UM3506 implements USB PD Protocol layer functions:

- Data encapsulation and extraction
- Hardware based *GoodCRC* response and automated retries
- Hard reset, Cable reset
- TX and RX buffer management
- Support PD packet capture mode
- Scalable and upgradable PD3.0 with PPS firmware support
  - PE (Policy Engine)
  - DPM (Device Policy Manager)
  - VDM message
  - Standard and vendor-specific power profile

DP/DM

The USB PD block contains two pairs of DP/DM pins for charging detection to detect conventional battery chargers which include BC1.2 and QC, AFC etc.

ADC

The USB PD block contains one multiple channel 12-bit SAR ADCs for analog to digital conversions.

The 12-bit analog-to-digital converter has up to 16 channels and performs conversions in single-shot or scan modes. Part of GPIO inputs can be connected to the global analog multiplex busses through a switch at each GPIO that can enable that GPIO to be connected to the mux bus for ADC use.

The CC1 and CC2 pins of both Type-C ports are not available to connect to the mux busses.

Low-side CSA

The USB PD block contains also integrates low-side current sense amplifier that is capable of detecting current in the order of 100 mA across a 5 mΩ external resistor. It also supports constant current mode of operation in power adapter application as a provider.

TL431 VBUS Regulator

The UM3506 device also integrates an TL431-based integrated feedback control circuitry in AC/DC applications for secondary side control with analog regulation of the VFB/CATH pins to achieve the appropriate voltage on VBUS as per the negotiated contract with the peer device over Type-C.

2.4. Peripherals

The UM3506 device equips with extensive peripherals.

UART

The UM3506 device embeds two UARTs. UART0 supports full modem control and RS-485/9-bit mode and allows both software address detection and automatic hardware address detection using 9-bit mode.

The UART interfaces can be served by the DMA controller.

I2C

The UM3506 device embeds up to two I2C interfaces can operate in multi-master or slave modes. Both can support Standard mode (up to 100 kbit/s) and Fast mode (up to 400 kbit/s) and Fast Mode Plus (up to 1 Mbit/s) with 20 mA output drive. They can also provide hardware support for SMBUS 2.0 and PMBUS 1.1.

SPI

The UM3506 device embeds one SPI controller. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer.

The SPI interfaces can be served by the DMA controller.

PWM

The UM3506 device embeds a PWM generator which support independent mode. It can support up to 6 independent channels, the 6 independent channels can be used for: output compare, PWM generation (edge or center-aligned modes) and one-pulse mode output. It also supports 3 pair complementary PWM outputs with programmable inserted dead times in the same multiplexed PINs.

GPIO

The UM3506 device provides 32 General Purpose I/O pins shared with other function pins depending on the chip configuration. The 32 pins are arranged in 2 ports named as P0, P1,

Each of the 32 pins is independent and has the corresponding register bits to control the pin mode function and data.

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions.

2.5. Low Power

UM3506 support normal work mode and low power sleep mode. It only support only clock gating and logic reset, no power gating. Enter sleep mode is configured by software. In sleep mode, flash, ADC, PLL will enter power-down mode. Only ROSC (4MHz) clock is running. Except AON_LPM module is active, all the other modules, including MCU core is under reset, and clock is gate-off.

In sleep mode, any GPIO's toggle or CC IO toggle event will wake up the chip.

- Support clock gating for low power
- Support timer-based and event-based sleep and wakeup
- Support wakeup based on Interface/Pin monitor
- Support wakeup based on Plug in/out

2.6. Clock System

UM3506 has one ROSC to generate 4 MHz clock, which works as both the sleep clock and also the PLL's input reference clock. PLL is used to generate the 132 MHz clock, which is used by SPI flash interface logic.

PWM clock is 66 MHz which is PLL clock divided by 2. MCU core and other system logic work at 33 MHz, which is the 132 MHz PLL clock divided by 4.

Internal RC oscillator

The IRC may be used as the clock source for the WDT, and/or as the clock that drives the PLL and subsequently the CPU. The nominal IRC frequency is 4MHz. The IRC is trimmed to 1 % accuracy over the entire voltage and temperature range.

Upon power-up or any chip reset, the device uses the IRC as the clock source. Software may later switch to one of the other available clock sources.

System PLL

The PLL accepts an input clock frequency of 4MHz. The input frequency is multiplied up to a high frequency with a Current Controlled Oscillator. The multiplier can be an integer value from 1 to 32. The CCO operates in the range of 156MHz to 320MHz, so there is an additional divider in the loop to keep the CCO within its frequency range while the PLL is providing the desired output frequency. The output divider may be set to divide by 2, 4, 8, or 16 to produce the output clock. The PLL output frequency must

be 133MHz. Since the minimum output divider value is 2, it is insured that the PLL output has a 50 % duty cycle. The PLL is turned off and bypassed following a chip reset and may be enabled by software. The program must configure and activate the PLL, wait for the PLL to lock, and then connect to the PLL as a clock source.

The PLL settling time is 100 us.

2.7. Power System

UM3506 integrate power regulator function block used to provide necessary voltage inside the chip which include core voltage 1.8V, digital interface voltage (3.3V) and CC interface voltage (1.125V).

UM3506 can operate from two possible external supply sources: VBUS_IN (3.0V~24V) or VDD33 (2.7V~3.3V). When powered through VBUS_IN, the internal regulator generates VDD33 (3.3V) for chip operation. The regulated supply, VDD, is either used directly inside some analog blocks or further regulated down to VDD18 (1.8V), which powers majority of the core using the regulator.

The power system provides assurance that voltage levels are as required for each respective mode and either delay mode entry (on power-on reset (POR), for example) until voltage levels are as required for proper function or generate resets BOD (brown-out detect) or interrupts LVD (low voltage detect).

2.8. Programming

The UM3506 on-chip Flash memory can be programmed using in-circuit programming or in-application programming.

The in-circuit programming (ICP) method is used to update the entire contents of the Flash memory, using the JTAG protocol or the boot loader to load the user application into the microcontroller. ICP offers quick and efficient design iterations and eliminates unnecessary package handling or socketing of devices.

In contrast to the ICP method, in-application programming (IAP) can use any communication interface supported by the microcontroller (UART, I2C, SPI, CC etc.) to download programming data into memory. IAP allows the user to re-program the Flash memory while the application is running. Nevertheless, part of the application has to have been previously programmed in the Flash memory using ICP.

The Flash interface implements instruction access and data access based on the AHB protocol. It implements a pre-fetch buffer that speeds up CPU code execution. It also implements the logic necessary to carry out Flash memory operations (Program/Erase). Program/Erase operations can be performed over the whole product voltage range. Read/Write protections and option bytes are also implemented.

- UM Private flash programmer
- XMODEM
- SPI/I2C/CC

3. Pin Information

3.1. Pin Assignment

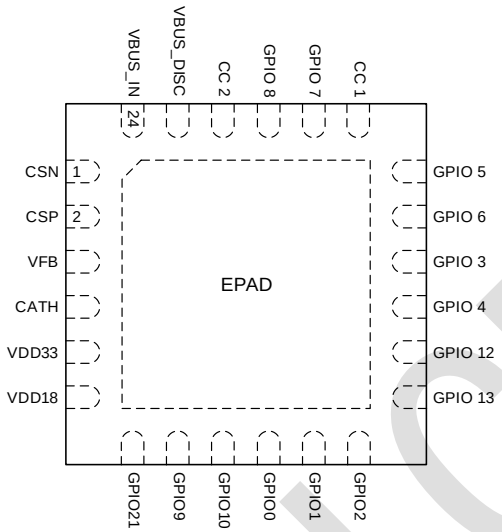


Figure 3-1: QFN24 Pin Map (Top View)

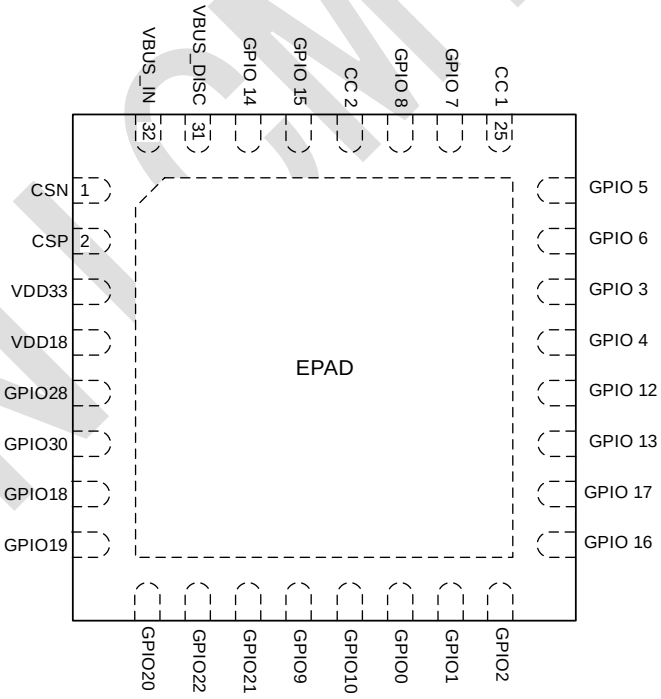


Figure 3-2: QFN32 Pin Map (Top View)

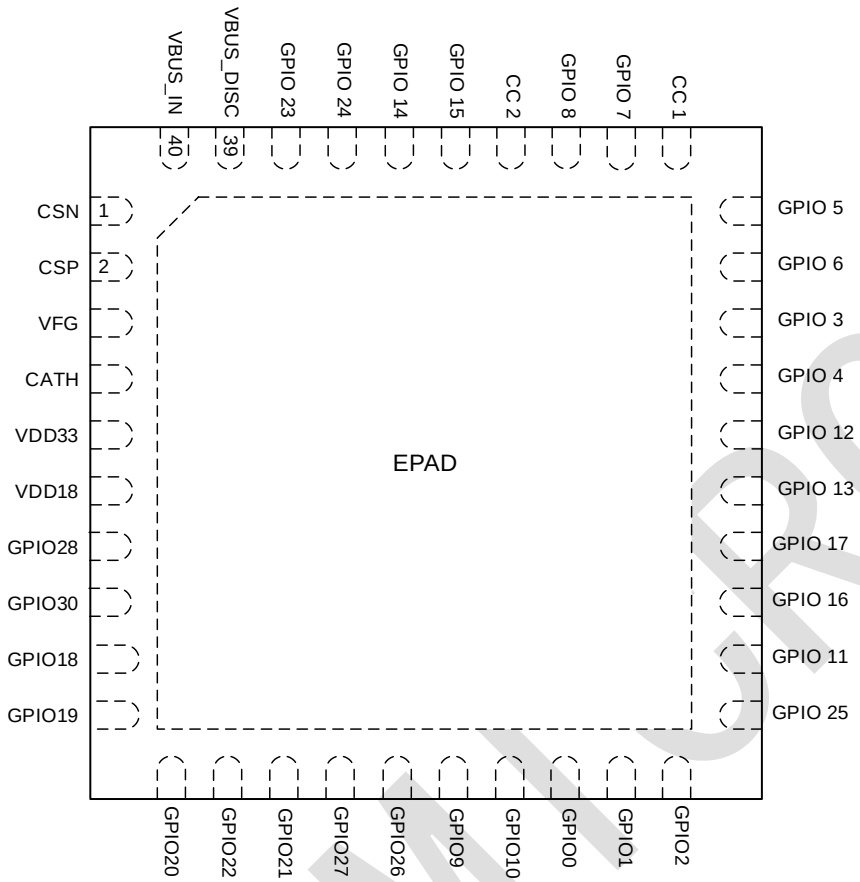


Figure 3-3: QFN40 Pin Map (Top View)

3.2. Pin List

Table 3-1: Pin List

QFN24	QFN32	*QFN40*	Pin	I/O	Description
1	1	*1*	CSN		Current sense negative
2	2	*2*	CSP		Current sense positive, ADC6
3	--	*3*	VFB		Voltage regulation feedback pin
4	--	*4*	CATH		Cathode of voltage regulation
5	3	*5*	VDD33		VDD33 Output
6	4	*6*	VDD18		VDD18 Output
--	5	*7*	GPIO28		GPIO28
--	6	*8*	GPIO30		GPIO30
--	7	*9*	GPIO18		GPIO18/I2C1_SCL, ADC10
--	8	*10*	GPIO19		GPIO19/I2C1_SDA/SPI_SSN2/SPI_SLV_SSN/JTAG_TCK, ADC9
--	9	*11*	GPIO20		GPIO20/ SPI_SCK/JTAG_TMS
--	10	*12*	GPIO22		GPIO22/ SPI_MOSI/JTAG_TDO

QFN24	QFN32	*QFN40*	Pin	I/O	Description
7	11	*13*	GPIO21		GPIO21/ SPI_MISO/JTAG_TDI
--	--	*14*	GPIO27		GPIO27
--	--	*15*	GPIO26		GPIO26
8	12	*16*	GPIO9		GPIO9/I2C0_SCL, *BIST_TDO*
9	13	*17*	GPIO10		GPIO10/I2C0_SDA, *BIST_TDI*
10	14	*18*	GPIO0		GPIO0/PWM2
11	15	*19*	GPIO1		GPIO1/PWM3
12	16	*20*	GPIO2		GPIO2 *GPIO0/1/2 (keep low when power on，change after power on)
--	--	*21*	GPIO25		GPIO25
--	--	*22*	GPIO11		GPIO11
--	17	*23*	GPIO16		GPIO16/SPI_SSN0, ADC12
--	18	*24*	GPIO17		GPIO17/SPI_SSN1, ADC11
13	19	*25*	GPIO13		GPIO13/UART0_RTS/UART1_TXD, ADC13
14	20	*26*	GPIO12		GPIO12/UART0_CTS/UART1_RXD, ADC14
15	21	*27*	GPIO4		GPIO4/PWM1, ADC15
16	22	*28*	GPIO3		GPIO3/PWM0, ADC8
17	23	*29*	GPIO6/DP1		GPIO6/DP1, ADC4
18	24	*30*	GPIO5/DM1		GPIO5/DM1, ADC5
19	25	*31*	CC1		CC1
20	26	*32*	GPIO7/DM0		GPIO7/UART0_TXD/DM0, ADC3
21	27	*33*	GPIO8/DP0		GPIO8/UART0_RXD/DP0, ADC2
22	28	*34*	CC2		CC2
--	29	*35*	GPIO15		GPIO15/PWM5
--	30	*36*	GPIO14		GPIO14/PWM4
--	--	*37*	GPIO24		GPIO24
--	--	*38*	GPIO23		GPIO23
23	31	*39*	VBUS_DISC		VBUS DISCHARGE, ADC7
24	32	*40*	VBUS_IN		VBUS VOLTAGE INPUT
25	33	*41*			***EPAD (ON THE BOTTOM)***

Notes：

A –Analog Signal; D –Digital Signal; I – Input; O – Output; G – Ground; P – Power; HZ –.

(QFN40: unavailable)

4. Electrical Characteristics

4.1. Absolute Maximum Ratings

Table 4-1: Absolute Maximum Ratings

Symbol	Description	Min.	Typical	Max.	Unit
VBUS_IN (VCC)	Power supply	-0.3	-	26	V
VDDIO	GPIO power supply	-0.3	-	3.8	V
VIO_GPIO	GPIO input voltage	-0.3	-	6	V
VIO_CC	CC RDB VCONN input voltage	-0.3	-	6	V
T_J	Operating junction temperature	–40	-	125	°C
T_{stg}	Storage temperature	–55	-	150	°C

4.2. ESD Ratings

Table 4-2: ESD Ratings

	Description	Value	Unit
V(ESD) Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22- V C101	±500	V

4.3. Recommended Operation Condition

Table 4-3: Recommended Operation Condition

Symbol	Description	Min.	Typical	Max.	Unit
Power					
VBUS_IN (VCC)	Power supply	3.3		24	V
VDDO33	Internal 3.3V LDO output	3.14	3.3	3.46	V
VDDO18	Internal 1.8V LDO output	1.71	1.8	1.89	V
Thermal					
TJ	Operating junction temperature	–40	-	125	°C
Tstg	Storage temperature	–55	-	150	°C
GPIO Characteristic					
VOH	High level output voltage	2.4			V
VOL	Low level output voltage			0.4	V
VIH	Input high voltage	2.0		3.9	V
VIL	Input low voltage	-0.3		0.8	V
RPU	Input pull-up 1K resistance	0.85	1.15	1.72	KOhm

Symbol	Description	Min.	Typical	Max.	Unit
	Input pull-up 10K resistance	8.48	10.5	12.9	KOhm
	Input pull-up 100K resistance	58.3	106.1	269.1	KOhm
RPD	Input pull-down resistance	54.2	103.2	241.7	KOhm
Iin	Input leakage current	-1		1	μA
	Input leakage current with 100K pull up	11	31	62	μA
	Input leakage current with 100K pull down	12	35	67	μA
IO	Tri-state output leakage current	-1		1	μA
PD BMC PHY					
VIO_CC	CC RDB VCONN input voltage	-0.3		5.5	V
ICS	Standard USB		80		μA
	USB 1.5A		180		μA
	USB 3A		330		μA
Rd	Pull down resistance	4.8	5.1	5.4	KOhm
PD_BITRATE	Data rate	270	300	330	Kbps
zDRIVER	TX output impedance	33		75	ohm
Trise	Tx rise time	300			ns
Tfall	Tx fall time	300			ns
VTRrx	VRXTR Rx Receive Rising Input threshold	0.46	0.51	0.56	V
VTFrx	VRXTR Rx Receiver falling Input threshold	0.56	0.61	0.66	V
VFRS	Fast Role Swap request voltage detection threshold		0.5		V
RFRS	Fast Role Swap request transmit driver resistance			5	ohm
USB quick charge interface DP,DM					
VOH	High level output voltage	2.4			V
VOL	Low level output voltage			0.4	V
VIH	Input high voltage				V
VIL	Input low voltage				V
RD-	D- pull down resistor	14.25	19.53	24.8	Kohm
RDCP_DAT	DCP D+/D- loopback resistance		20		ohm
Power on Reset					
TD	Reset delay time		300		us
OSC/PLL					
Fosc	OSC output frequency		4		MHz
FPLL	PLL output frequency		132		MHz
TLOCK	PLL lock time		500		us
DPLL	PLL output duty cycle	40		60	%
Jitter	PLL clock cycle-to-cycle Jitter	-100		100	ps
Fsys	System clock		33		MHz
Fflash	Flash interface clock		66		MHz

Symbol	Description	Min.	Typical	Max.	Unit
CSA					
Gain	Current sense block gain		15/30		
PWM					
FPWM	Operating frequency			Fflash	MHz
ADC					
Resolution	ADC Resolution		12		bit
INL	Integral non-linearity	-4		4	LSB
DNL	Differential non-linearity	-3		3	LSB
SR	Sample rate			250	KSPS
CATH					
IKA	Current on cath pin			10	mA
IIDAC	Internal DAC output current	-12.8		100	uA
UART					
FUART				11	Mbps
I2C					
FI2C	Bit rate			11	Mbps
SPI					
FSPI	SPI Operating frequency			16	MHz

Notes：

The speed is only the line speed not the interface processing speed.

4.4. Thermal Information

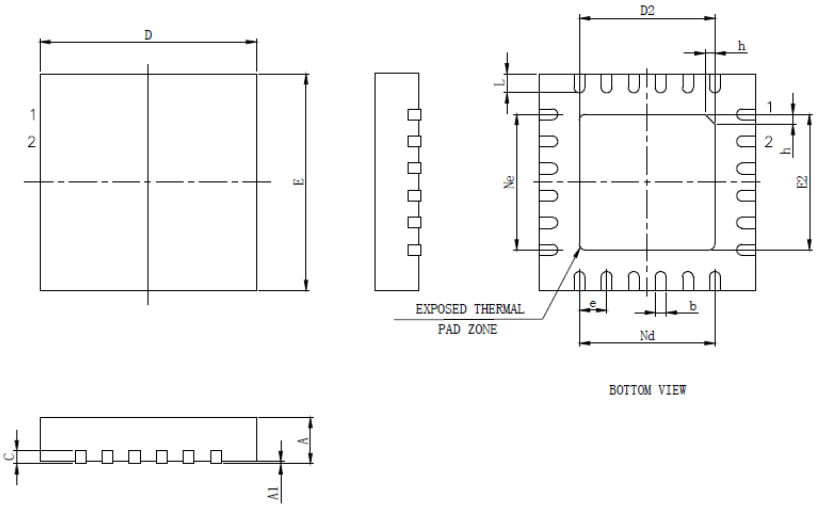
Condition: (TA)=25℃,VDD=3.3V 和 VDDD18=1.8V

Table 4-4: Thermal Information

Thermal	Description	Value	Unit
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	49.1	˚C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	28.1	˚C/W
$R_{\Theta JC}$	Junction-To-Case Thermal Resistance	15.7	˚C/W

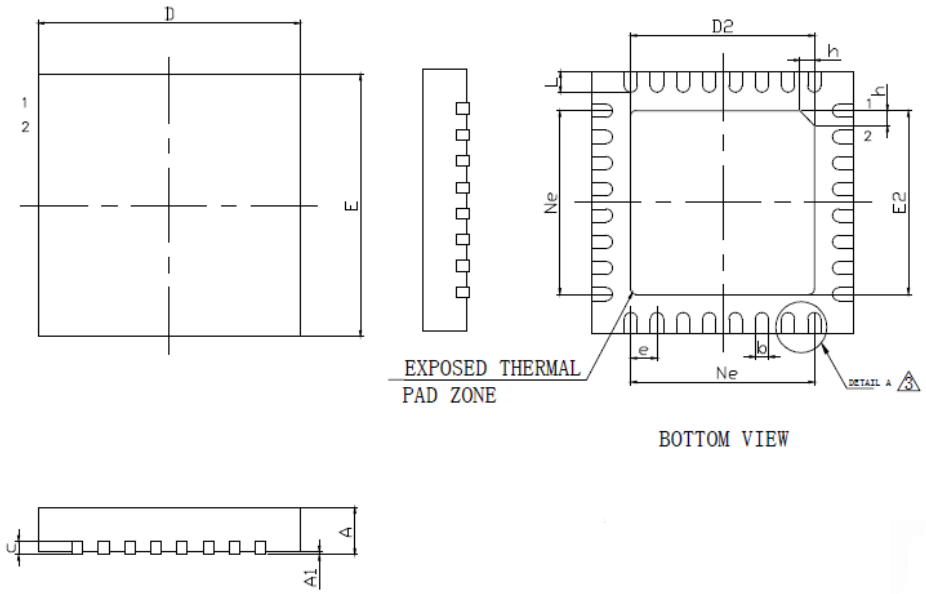
5. Package

5.1. QFN24 (4*4mm)



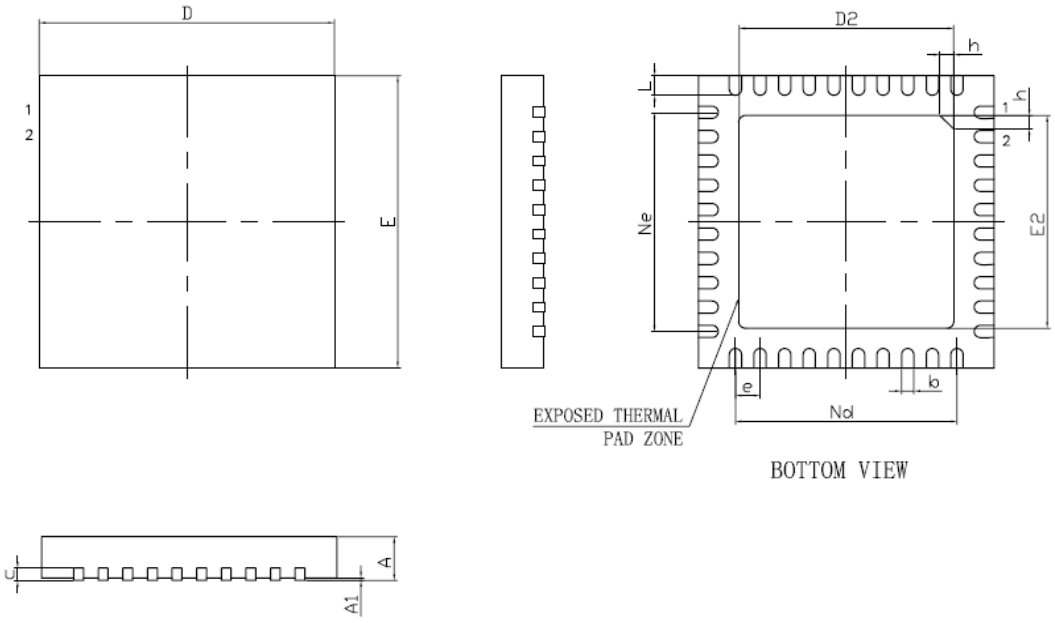
Symbol	Millimeter		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.40	2.50	2.60
e	0.50BSC		
Ne	2.50BSC		
Nd	2.50BSC		
E	3.90	4.00	4.10
E2	2.40	2.50	2.60
L	0.35	0.40	0.45
H	0.30	0.35	0.40

5.2. QFN32 (5*5mm)



Symbol	Millimeter		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	4.90	5.00	5.10
D2	3.40	3.50	3.60
e	0.50BSC		
Ne	3.50BSC		
E	4.90	5.00	5.10
E2	3.40	3.50	3.60
L	0.35	0.40	0.45
h	0.30	0.35	0.40

5.3. QFN40 (6*6mm)



Symbol	Millimeter		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	--	0.02	0.05
b	0.18	0.25	0.30
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.10	4.20	4.30
e	0.50BSC		
Ne	4.50BSC		
Nd	4.50BSC		
E	5.90	6.00	6.10
E2	4.10	4.20	4.30
L	0.35	0.40	0.45
h	0.30	0.35	0.40

6. Typical Application

UM3506 provide the following typical application.

- SRC port in Opto-feedback power adapter
- DRP port in Power Bank

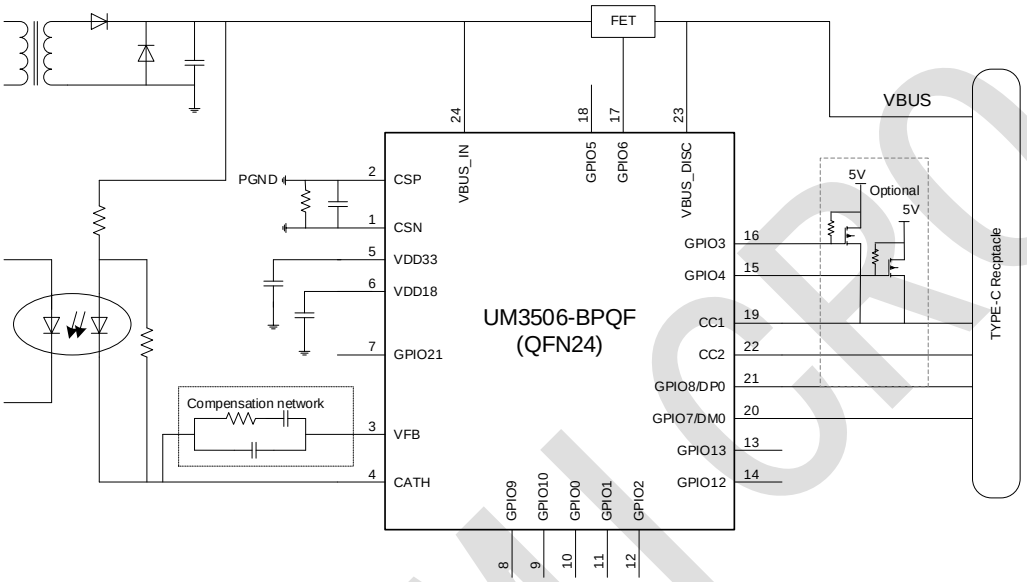


Figure 6-1: SRC Port Application in Power Adapter

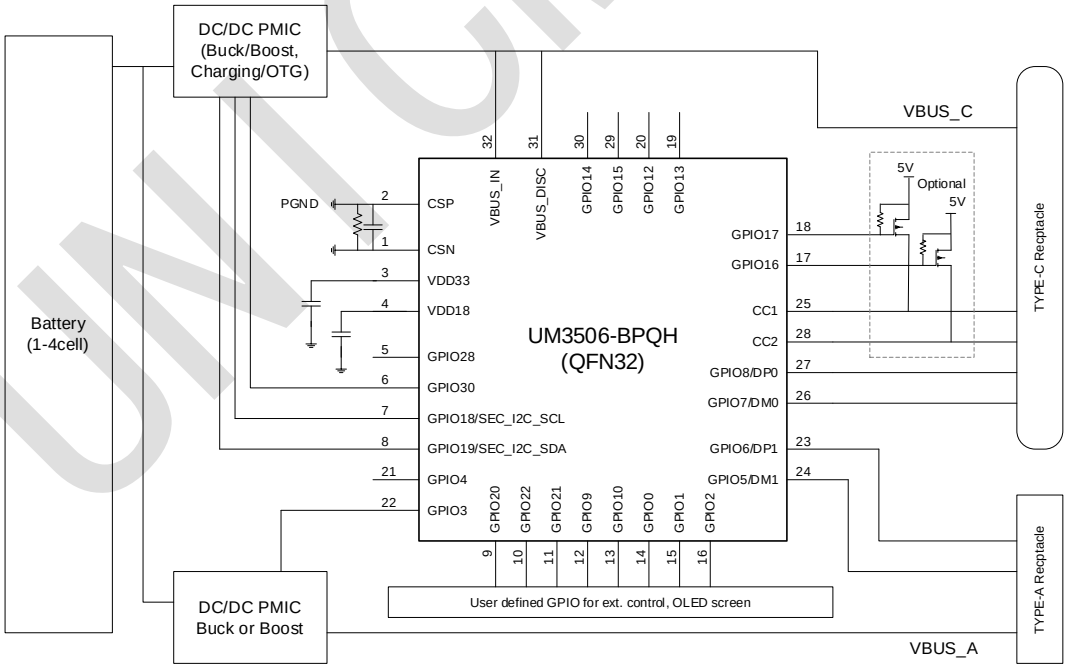


Figure 6-2: DRP Port Application in Power Bank

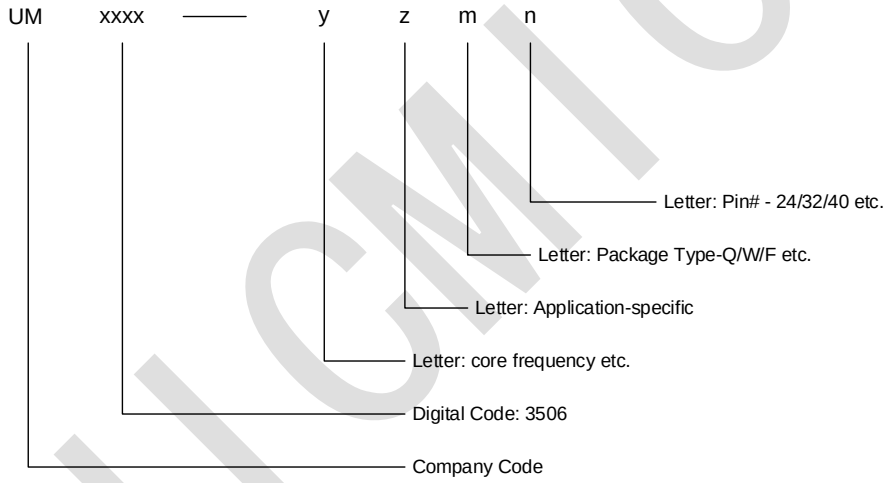
7. Order Information

UM3506 provide the following part number and application.

Table 7-1: Product Part Number

P/N	Application	Package
UM3506-BPQH	SRC/SNK/DRP	QFN, 32-Pin
UM3506-BPQF	SRC Only	QFN, 24-Pin
UM3506-BPQJ	*SRC/SNK/DRP*	*QFN, 40-Pin*
UM3506-BDQF	*SRC/SNK/DRP*	*QFN, 24-Pin*
UM3506-BNQF	*SNK Only*	*QFN, 24-Pin*

Product number code definitions.



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Revision History

Revision	Date	Author	Description
V1.0			Initial
…			
…			
V1.5.5	2022/12/5		Update SPI signal description
V1.5.6			Update
V1.5.7			Update